LV5692P, LV5693P

Multi Voltage Regulator IC Application Note

ON Semiconductor®

Overview

LV5692P/93P is a multiple voltage regulator for car audio system, which allows reduction of quiescent current. This IC has 5 systems of voltage regulator, pre-driver for Pch- FET which generates USB power and a high side switch for external devices.

The following protection circuits are integrated: overcurrent protector, overvoltage protector and Thermal Shut Down. This IC is suitable for use in car audio with USB port. The package is HZIP15J

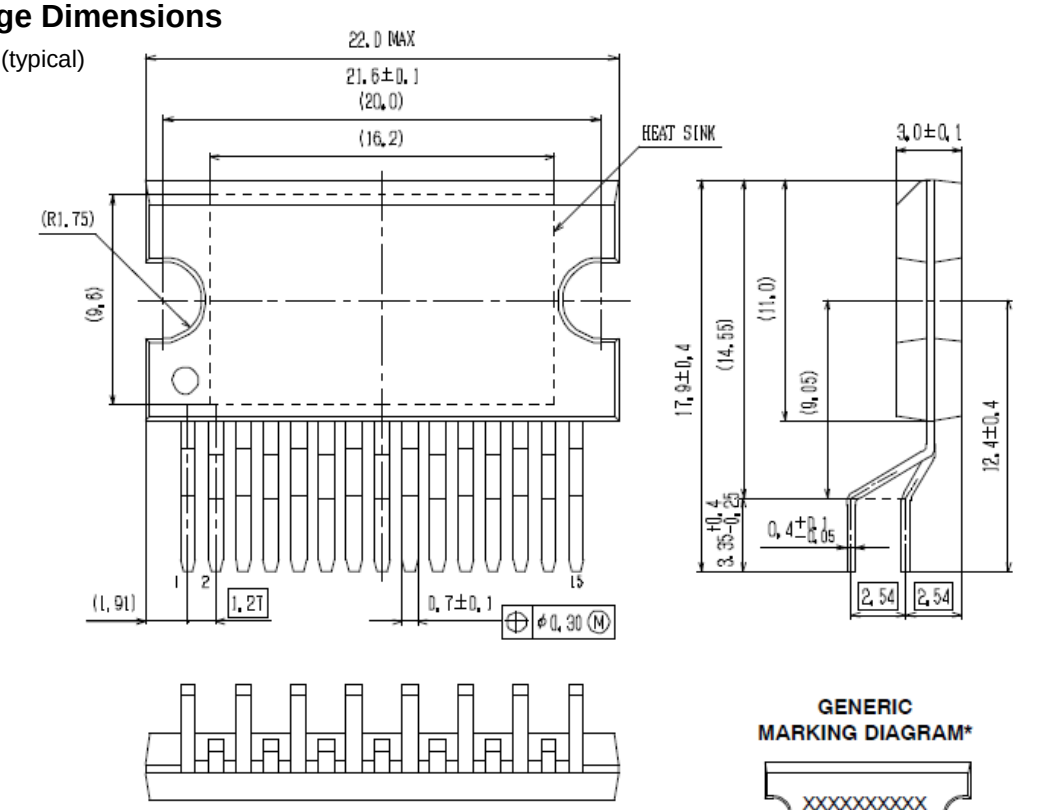
Functions

- Quiescent Current 50uA (Typ, when only VDD is in operation)
- 5 channel regulators and 1channel P-FET pre-driver (for USB-POWER)
  - For VDD: Vout is 3.3V(LV5692P),5.7V(LV5693P), Iomax is 300mA
  - For DSP: Vout is 3.3V, Iomax is 300mA
  - For CD: Vout is 8.0V, Iomax is 1300mA
  - For Ilumi: Vout is 8.4V, Iomax is 500mA
  - For Audio:Vout is 8.4V, Iomax is 500mA
  - For USB (Controller) , Vout is flexible (configurable with external resistor) , Iomax is 1000mA
- High-side switch :Voltage difference between input and output is 0.5V, Iomax is 500mA
- Overcurrent protector
- Overvoltage protector (Without VDD-OUT) *Detection voltage is 21V (typical)
- Thermal Shut Down *175°C (typical)

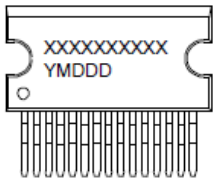
(Warning) The protector functions only improve the IC's tolerance and they do not guarantee the safety of the IC if used under the conditions out of safety range or ratings. Use of the IC such as use under over-current protection range or thermal shutdown state may degrade the IC's reliability and eventually damage the IC.

Package Dimensions

unit : mm(typical)



GENERIC MARKING DIAGRAM*



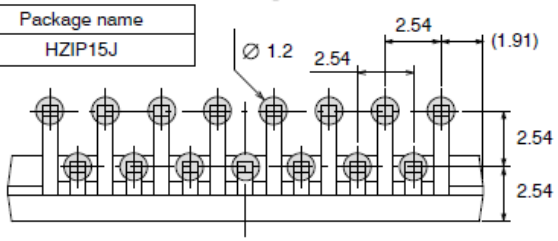
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

SOLDERING FOOTPRINT*

(Unit: mm) Through Hole Area

Package name
HZIP15J



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Fig1. Package Dimensions of HZIP15J

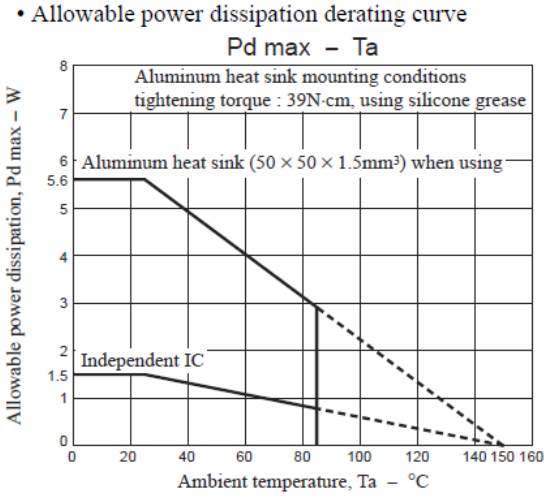


Fig2. Allowable Power Dissipation Derating Curve

Pin Assignment

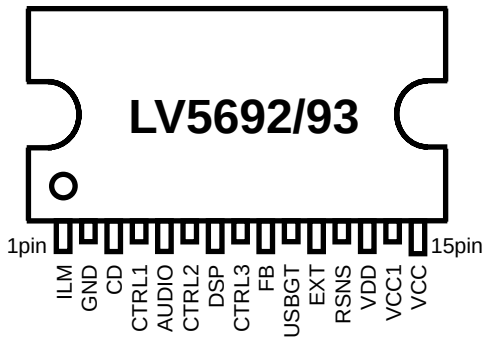


Fig3. Pin Assignment

Block Diagram

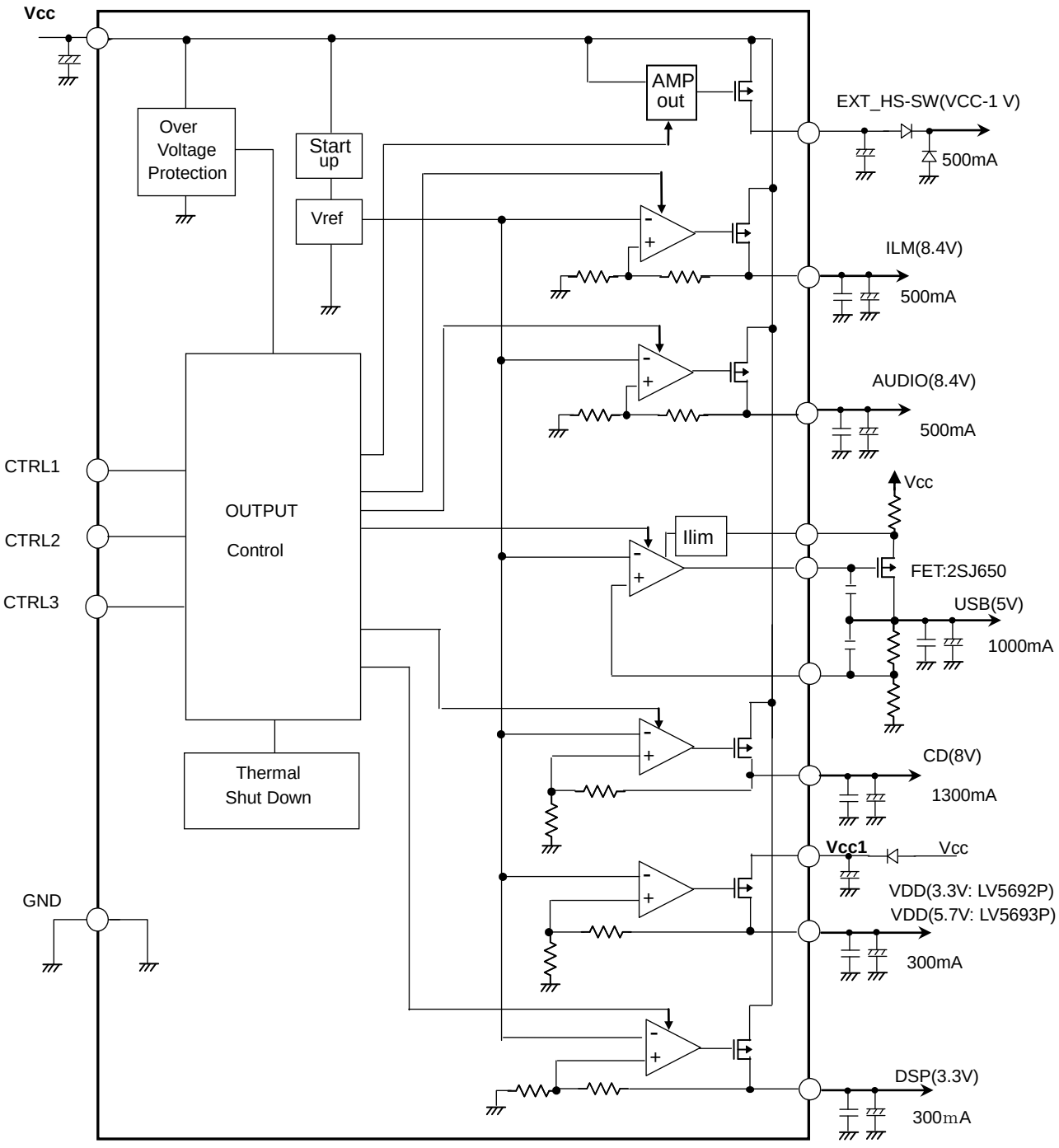


Fig4. Block Diagram

Specifications

Absolute Maximum Ratings at Ta=25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	Vcc max		36	V
Power dissipation	Pd max (*1)	・IC Unit ・At using Al heat sink of “50×50×1.5mm^3 ・At Infinite heat sink	1.5 5.6 32.5	W
Peak voltage	Vcc peak	・Regarding waveform, refer to below	50	V
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* 1: Ta≤25°C

・Peak Voltage testing pulse wave

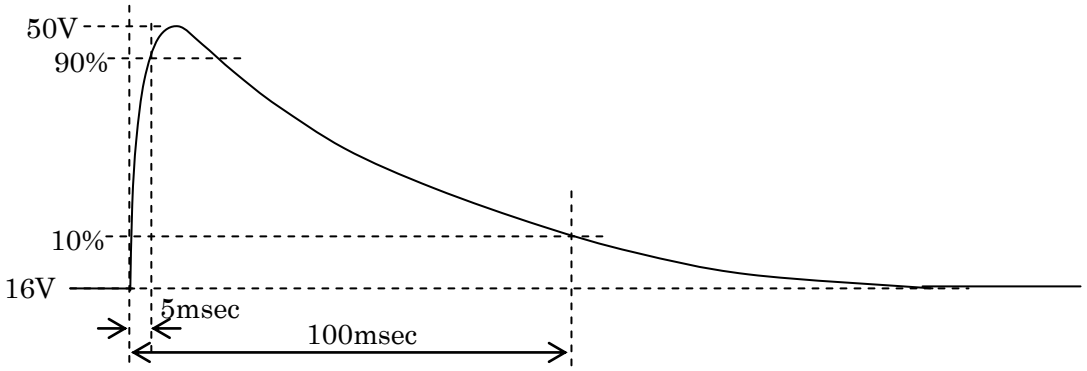


Fig5. Peak Voltage testing pulse wave

Recommended Operating Ranges at Ta=25°C

Parameter	Conditions	Rating	Units
Power supply voltage rating 1	VDD-OUT ON, DSP-OUT ON	LV5692P: 7 to 16 LV5693P: 7.7 to 16	V
Power supply voltage rating 2	ILM-OUT ON	10.8 to 16	V
Power supply voltage rating 3	AUDIO-OUT ON, CD-OUT ON	10 to 16	V

*VCC1 should be as follows: VCC1>VCC-0.7V

Electrical Characteristics Vcc=Vcc1=14.4V at Ta=25ºC (*2)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Quiescent Current	Icc	VDD: No Load,CTRL1/2/3="L/L/L"		50	100	μA
CTRL1 Input Voltage Level						
"L" Input voltage	$V_{IL}1$		0		0.3	V
"M" Input voltage	$V_{IM}1$		1.10	1.65	2.10	V
"H" Input voltage	$V_{IH}1$		2.50		5.50	V
Input impedance	$R_{IN}1$		280	400	520	kΩ
CTRL2 Input Voltage Level						
"L" Input voltage	$V_{IL}2$		0		0.3	V
"M1" Input voltage	$V_{IM1}2$		0.8	1.06	1.4	V
"M2" Input voltage	$V_{IM2}2$		1.90	2.13	2.40	V
"H" Input voltage	$V_{IH}2$		2.9	3.2	5.5	V
Input impedance	$R_{IN}2$		280	400	520	kΩ
CTL3 Input Voltage Level						
"L"Input voltage	$V_{IL}3$		0		0.3	V
"H" Input voltage	$V_{IH}3$		2.5		5.5	V
Input impedance	$R_{IN}3$		280	400	520	kΩ
VDD 3.3V OUT (LV5692P)						
Output Voltage	Vo1	Io1= 200 mA,	3.16	3.3	3.45	V
Output Current	Io1	Vo1≥3.1V	300			mA
Line regulation	$\Delta Vo_{LN}1$	7.5V<Vcc1<16 V, Io1= 200 mA		30	100	mV
Load regulation	$\Delta Vo_{LD}1$	1 mA<Io1<200 mA		70	150	mV
Ripple rejection	$R_{REJ}1$	f=120Hz, Io1= 200 mA	30	40		dB
VDD 5.7V OUT (LV5693P)						
Output Voltage	Vo1	Io1= 200 mA,	5.415	5.7	5.985	V
Output Current	Io1	Vo1≥5.35V	300			mA
Line regulation	$\Delta Vo_{LN}1$	8.2V<Vcc1<16 V, Io1= 200 mA		30	100	mV
Load regulation	$\Delta Vo_{LD}1$	1 mA<Io1<200 mA		70	150	mV
Dropout voltage1	$V_{DROP}1$	Io1= 200 mA		0.5	1.2	V
Dropout voltage 2	$V_{DROP}1'$	Io1= 100 mA		0.25	0.6	V
Ripple rejection	$R_{REJ}1$	f=120Hz, Io1= 200 mA	30	40		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Units
USB ; CTRL3="H" (External Pch-FET (2SJ650) , Resistors: 27kΩ, 9.1kΩ)						
Output Voltage	Vo2	Io2= 1000 mA	4.75	5	5.25	V
Output Current	Io2	Vo2≥4.75V	1000			mA
Line regulation	$\Delta Vo_{LN}2$	10 V<Vcc<16 V, Io2= 1000 mA		50	90	mV
Load regulation	$\Delta Vo_{LD}2$	10 mA<Io2<1000 mA		100	150	mV
Dropout voltage	$V_{DROP}2$	Io2= 1000 mA		1	1.5	V
Ripple rejection	$R_{REJ}2$	f=120Hz ,Io2= 1000 mA	40	50		dB
AUDIO (8.4V) OUT; CTRL1= "M or H"						
Output Voltage	Vo3	Io3= 400 mA	8.0	8.4	8.8	V
Output Current	Io3	Vo3≥8.0V	500			mA
Line regulation	$\Delta Vo_{LN}3$	10V<Vcc<16 V, Io3= 400 mA		30	90	mV
Load regulation	$\Delta Vo_{LD}3$	1 mA<Io3<400 mA		70	150	mV
Dropout voltage1	$V_{DROP}3$	Io3= 400 mA		0.4	0.8	V
Dropout voltage2	$V_{DROP}3'$	Io3= 200 mA		0.2	0.4	V
Ripple rejection	$R_{REJ}3$	f=120Hz, Io3=400 mA	40	50		dB
ILM (8.4V) OUT; CTRL2= "M1 or H"						
Output Voltage	Vo4	Io4= 400 mA	8.0	8.4	8.8	V
Output Current	Io4		500			mA
Line regulation	$\Delta Vo_{LN}4$	10.8V<Vcc<16 V, Io4= 400 mA		30	90	mV
Load regulation	$\Delta Vo_{LD}4$	1 mA<Io4<400 mA		70	150	mV
Dropout voltage1	$V_{DROP}4$	Io4= 400 mA		1.0	1.5	V
Dropout voltage2	$V_{DROP}4'$	Io4= 200 mA		0.7	1.05	V
Ripple rejection	$R_{REJ}4$	f=120Hz, Io4= 400 mA	40	50		dB
EXT_HS-SW; CTRL2= "M2 or H"						
Output Voltage	Vo5	Io5= 500 mA		Vcc -0.5	Vcc -1.0	V
Output Current	Io5	Vo5≤Vcc-1V	500			mA
DSP (3.3V) OUT; CTRL1= "M or H"						
Output Voltage	Vo7	Io7= 200 mA	3.1	3.3	3.5	V
Output Current	Io7		300			mA
Line regulation	$\Delta Vo_{LN}7$	10V<Vcc<16 V, Io7= 200 mA		30	90	mV
Load regulation	$\Delta Vo_{LD}7$	1 mA<Io4<200 mA		70	150	mV
Ripple rejection	$R_{REJ}7$	f=120Hz, Io4= 200 mA	40	50		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CD (8.0V) OUT; CTRL1="H"						
Output Voltage	Vo8	Io8= 1000 mA	7.6	8.0	8.4	V
Output Current	Io8		1300			mA
Line regulation	$\Delta Vo_{LN}8$	10.5V<Vcc<16 V, Io8= 1000 mA		50	100	mV
Load regulation	$\Delta Vo_{LD}8$	10 mA<Io8<1000 mA		100	200	mV
Dropout voltage	V_{DROP8}	Io8= 1000 mA		1.0	1.5	V
Ripple rejection	$R_{REJ}8$	f=120Hz ,Io8= 1000 mA	40	50		dB

*2: The entire specification has been defined based on the tests performed under the conditions where Tj and Ta (=25 ºC) are almost equal. These tests were performed with pulse load to minimize the increase of junction temperature (Tj).

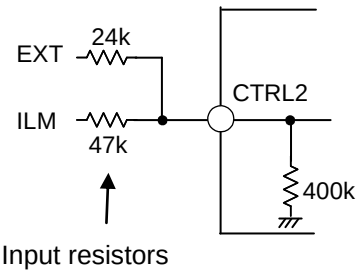
CTRL PINS TRUTH-VALUE TABLE

CTRL1	CD	DSP	Audio
L	OFF	OFF	OFF
M	OFF	ON	ON
H	ON	ON	ON

CTRL3	USB
L	OFF
H	ON

CTRL2	EXT	ILM
L	OFF	OFF
M1	OFF	ON
M2	ON	OFF
H	ON	ON

・CTRL2 Typical Application Circuit



EXT	ILM	CTRL2
0V	0V	0V
0V	3.3V	1.06V
3.3V	0V	2.13V
3.3V	3.3V	3.20V

Fig6. CTRL2 Application Circuit

Note) CTRL pins support input voltage of 3.3V. When 5V is supplied to the pins, change input resistor values.

(Warning) Usage of CTRL2

When CTRL pin transits between L and M2, since it passes M1, ILM is turned on for a moment. Likewise, when CTRL pin transits between H and M1, since it passes M2, ILM is turned off for a moment.

To avoid operation failure by the above factors, please refer to the following precautions.

* Do not connect parasitic capacitor to CTRL as much as possible.
* If use of capacitor for CTRL is required, keep the resistance value as low as possible.
* Make sure that the output load capacitor has enough margin against the voltage fluctuation due to instantaneous ON/OFF.

Timing Chart

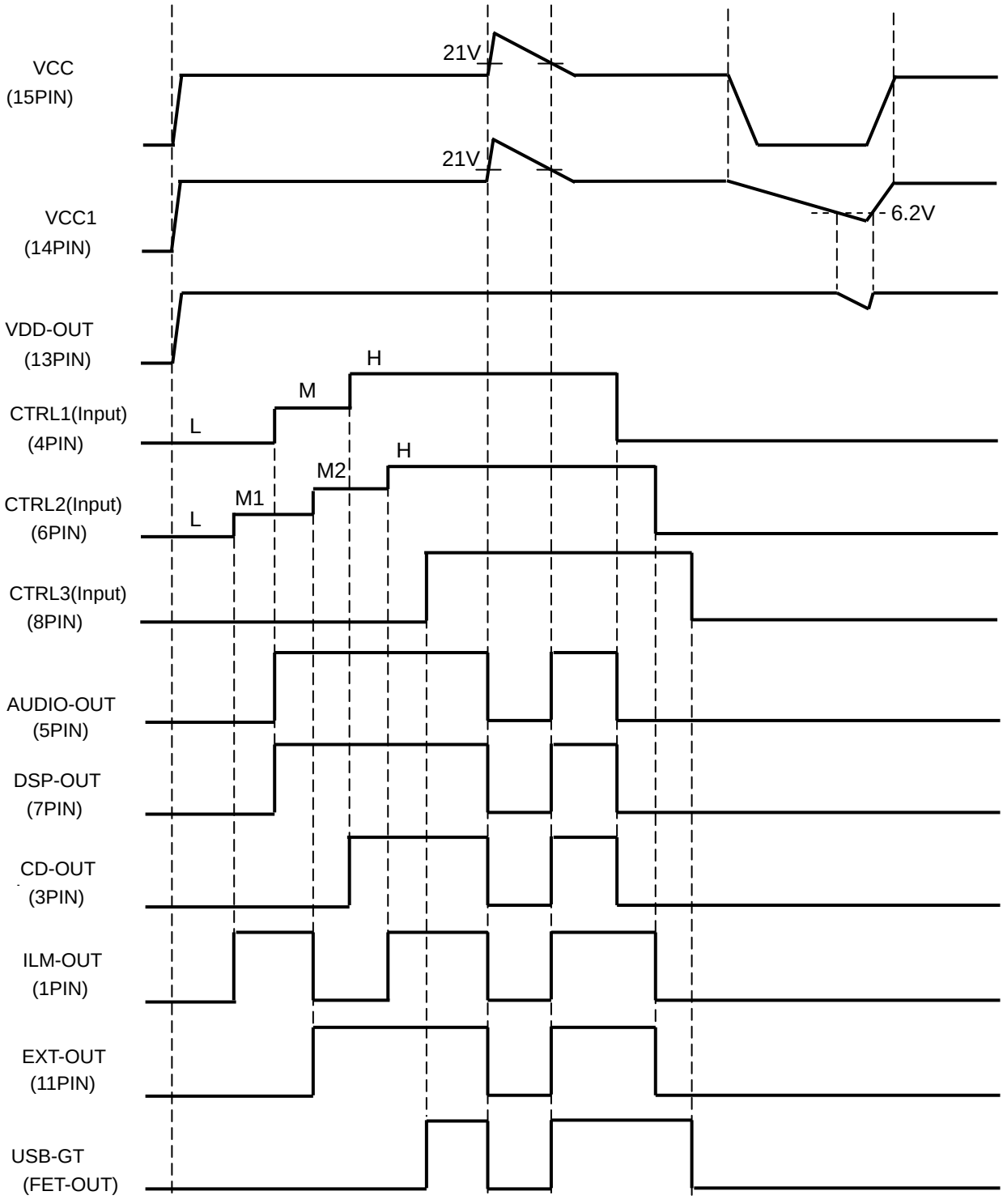


Fig7. Timing Chart

Typical Characteristics(LV5693P)

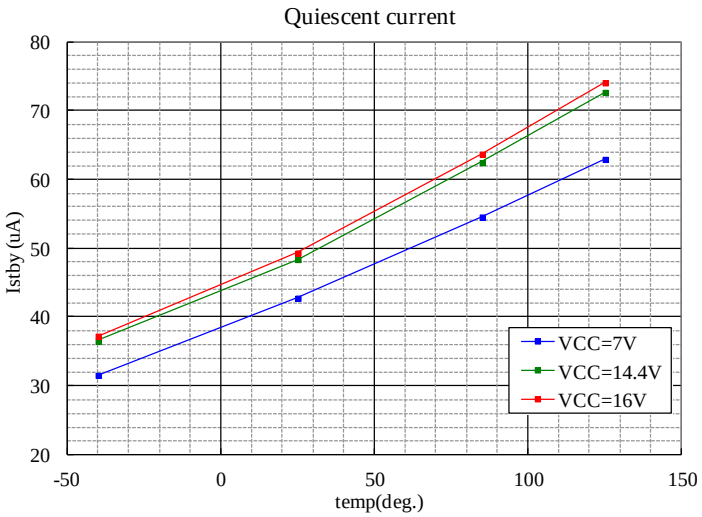


Fig8. Quiescent current vs Temperature

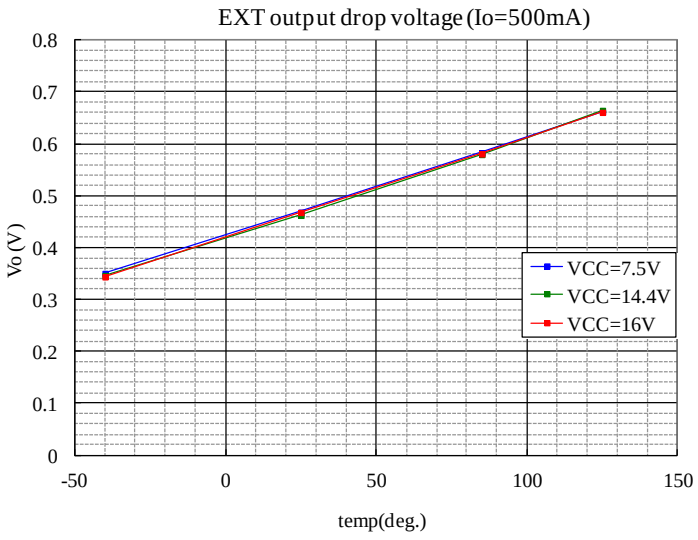


Fig9. EXT drop voltage vs Temperature

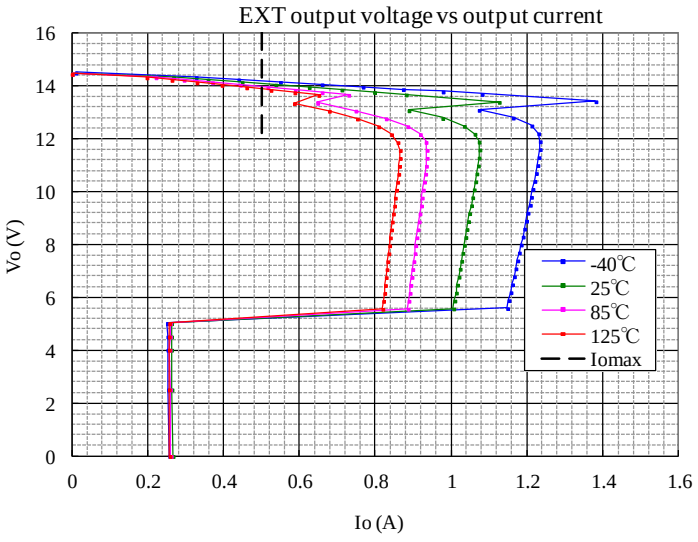


Fig10. EXT voltage vs current

In case of LV5692P, VDD output voltage is 3.3V typical.

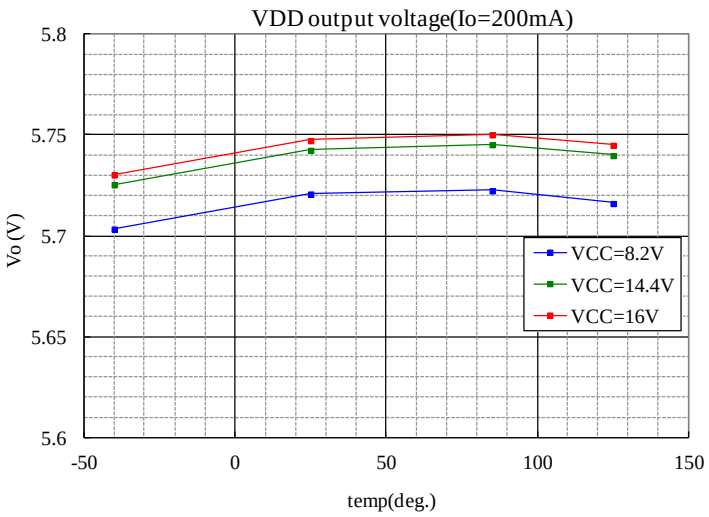


Fig11. VDD voltage vs Temperature

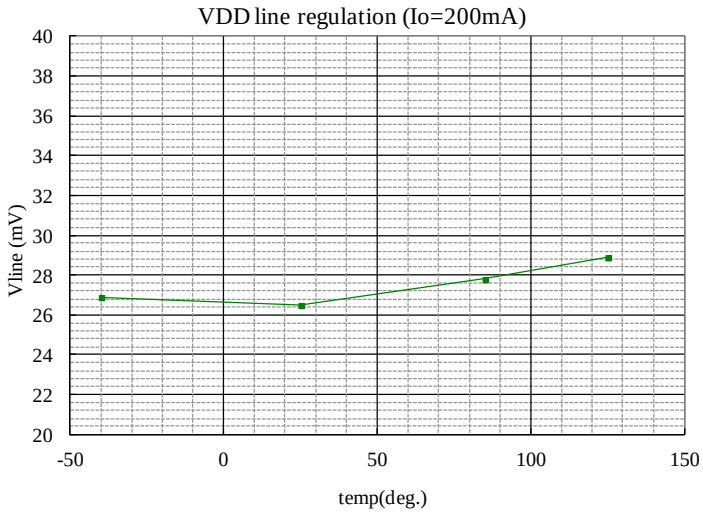


Fig12. VDD Line regulation vs Temperature

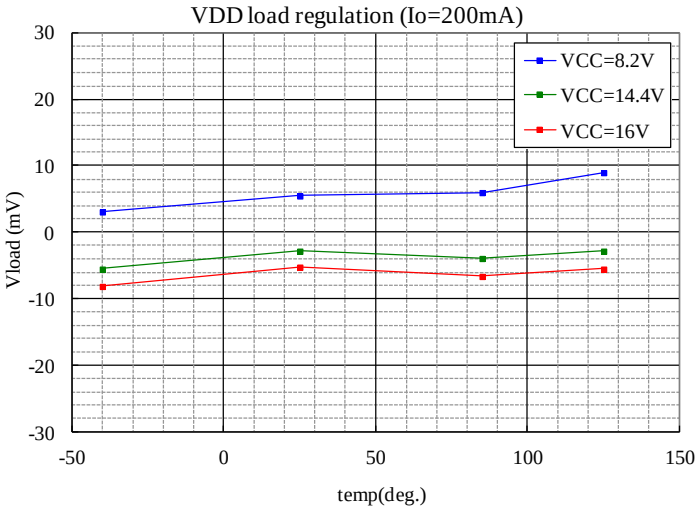


Fig13. VDD Load regulation vs Temperature

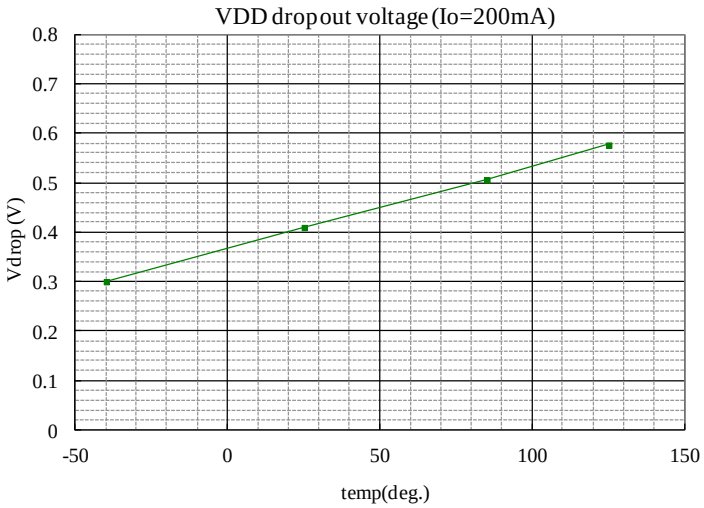


Fig14. VDD dropout voltage vs Temperature

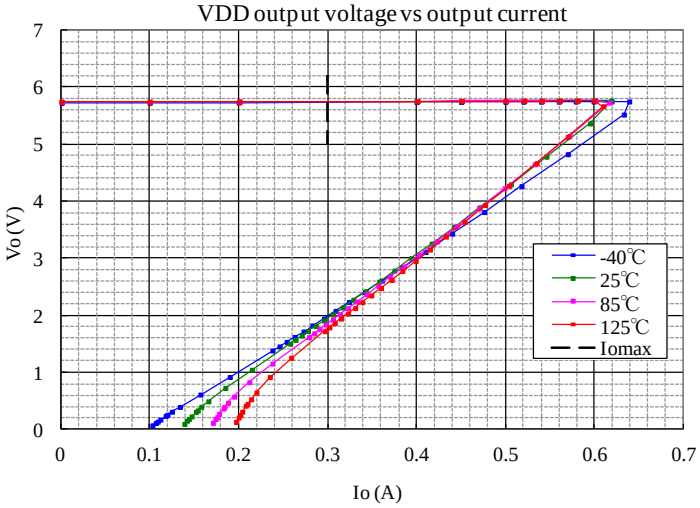


Fig15. VDD voltage vs current

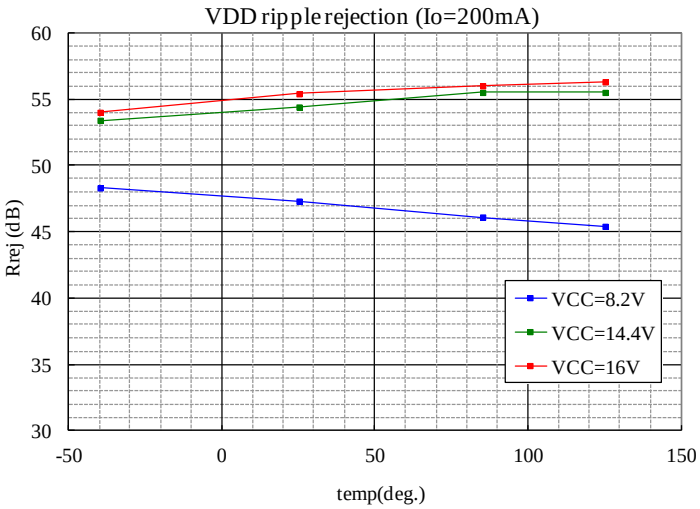


Fig16. VDD Ripple rejection vs Temperature

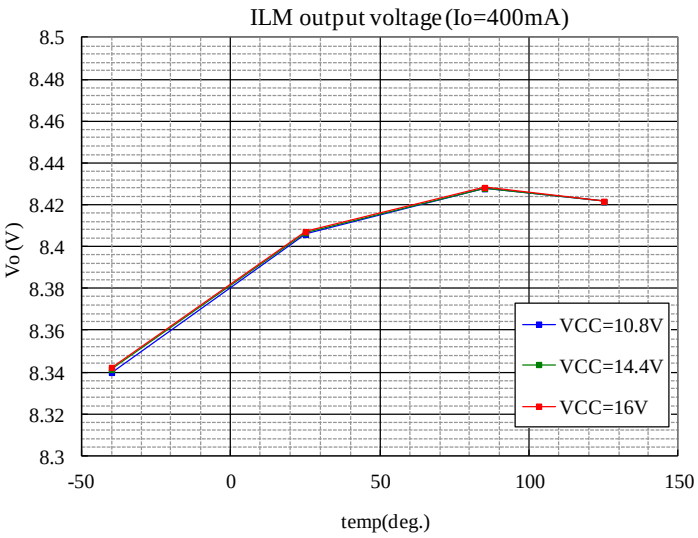


Fig17. ILM voltage vs Temperature

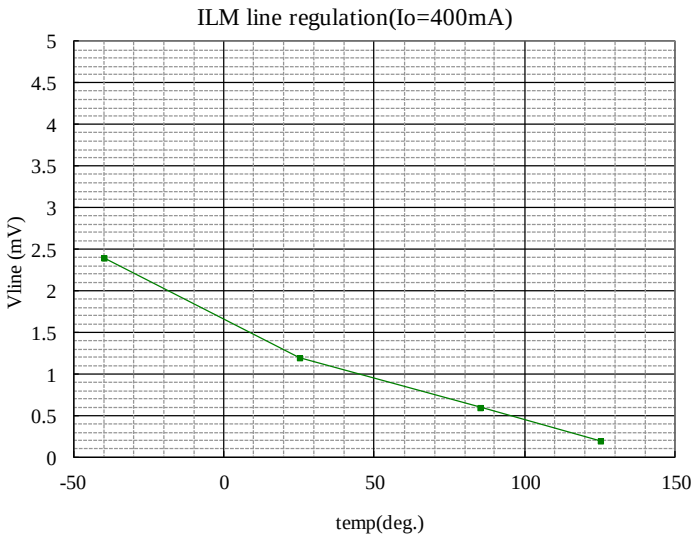


Fig18. ILM Line regulation vs Temperature

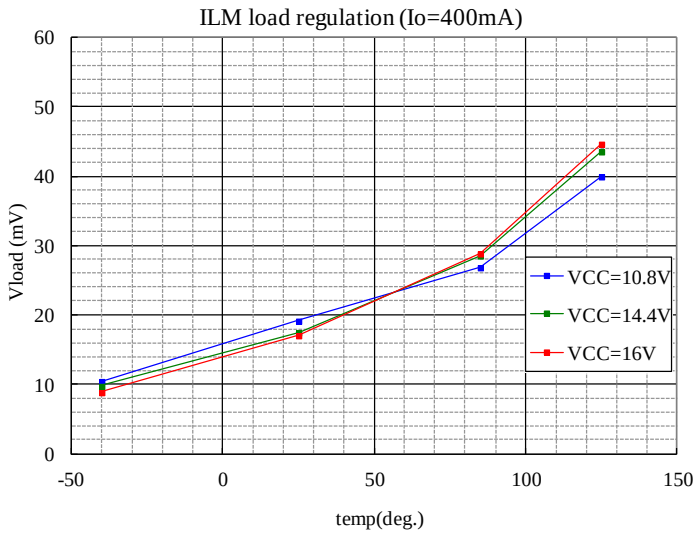


Fig19. ILM Load regulation vs Temperature

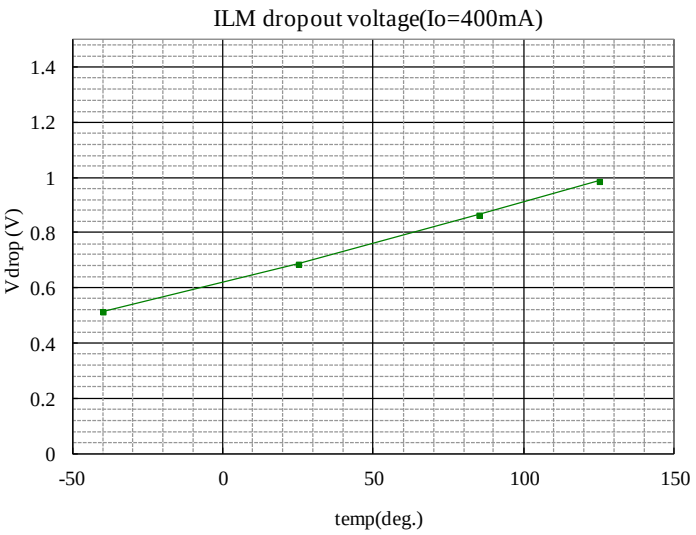


Fig20. ILM dropout voltage vs Temperature

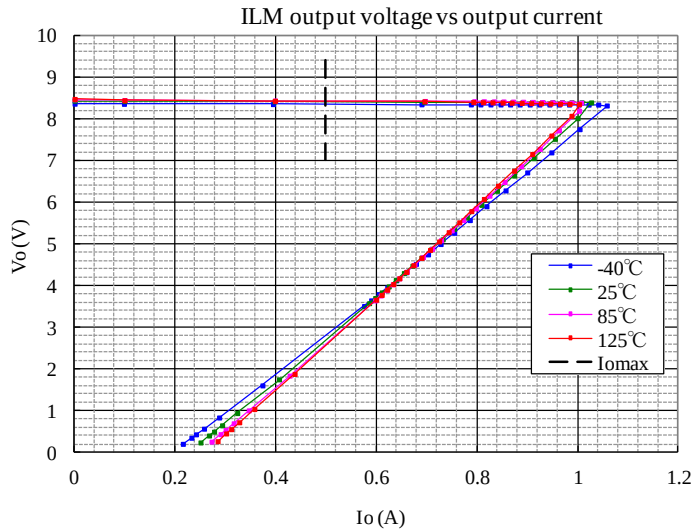


Fig21. ILM voltage vs current

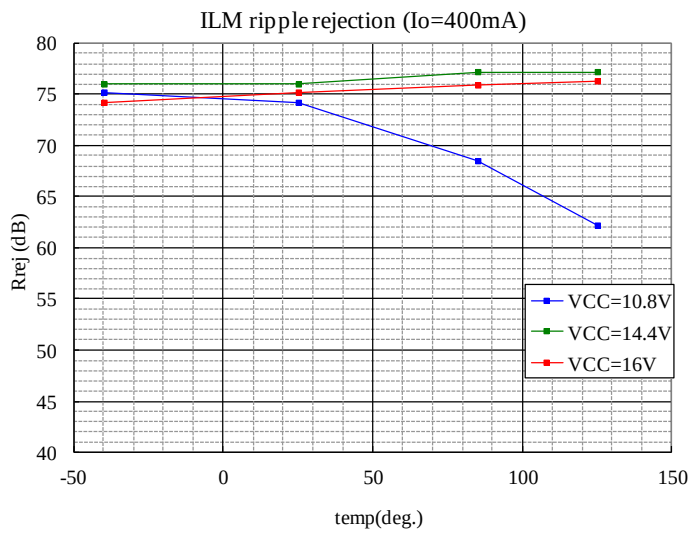


Fig22. ILM Ripple rejection vs Temperature

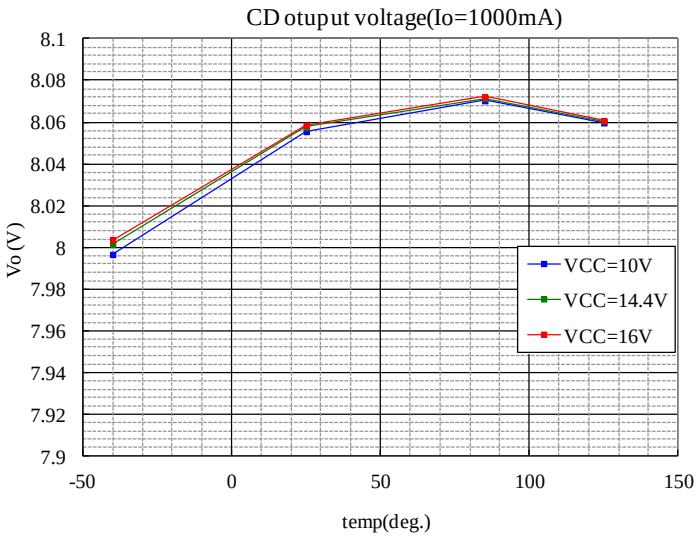


Fig23. CD voltage vs Temperature

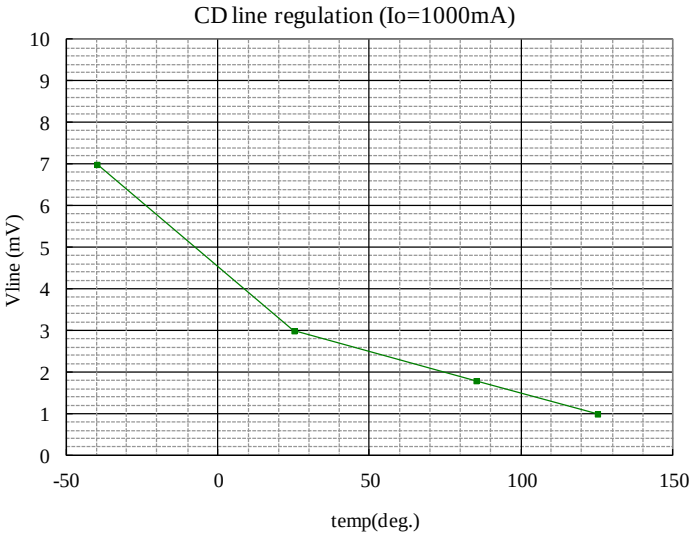


Fig24. CD Line regulation vs Temperature

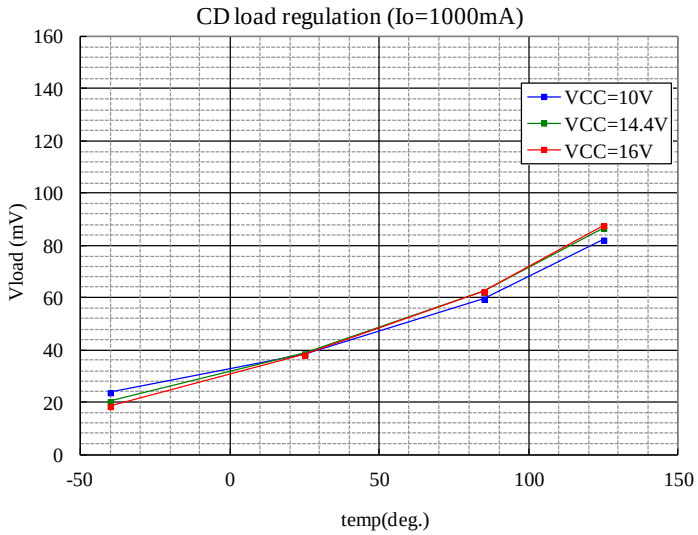


Fig25. CD Load regulation vs Temperature

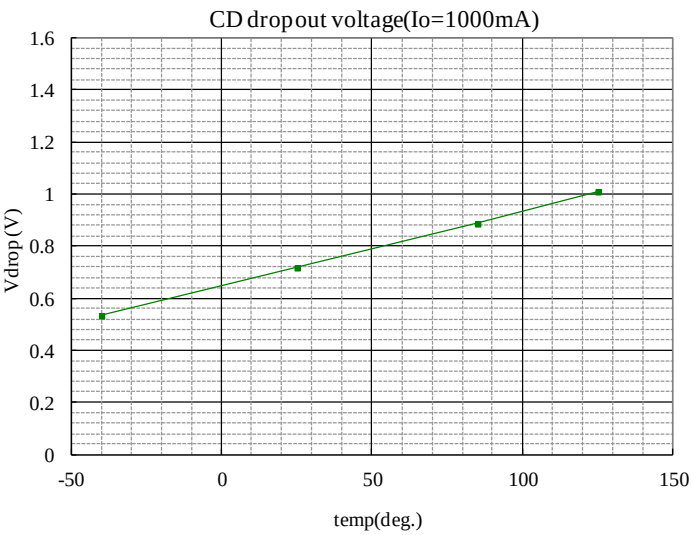


Fig26. CD dropout voltage vs Temperature

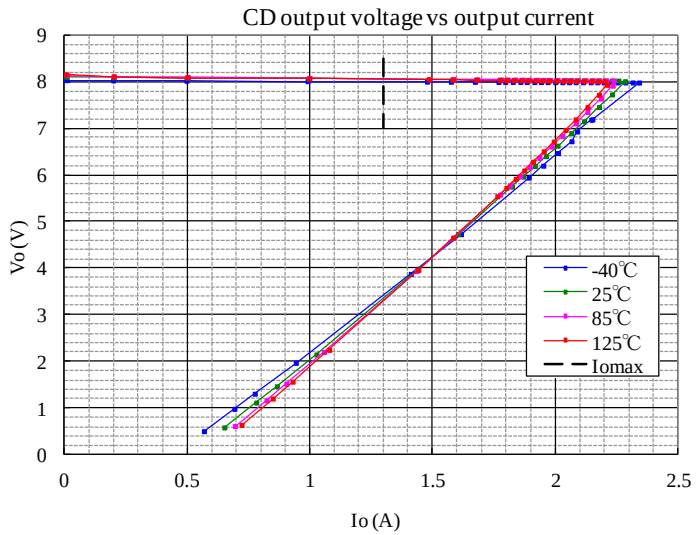


Fig27. CD voltage vs current

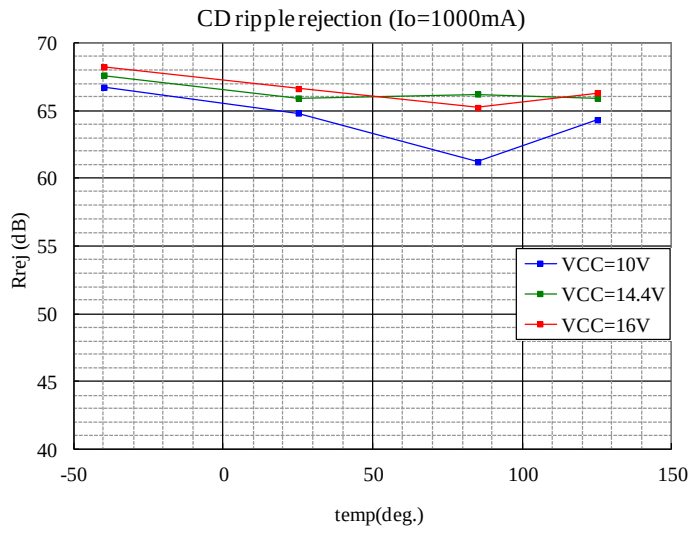


Fig28. CD Ripple rejection vs Temperature

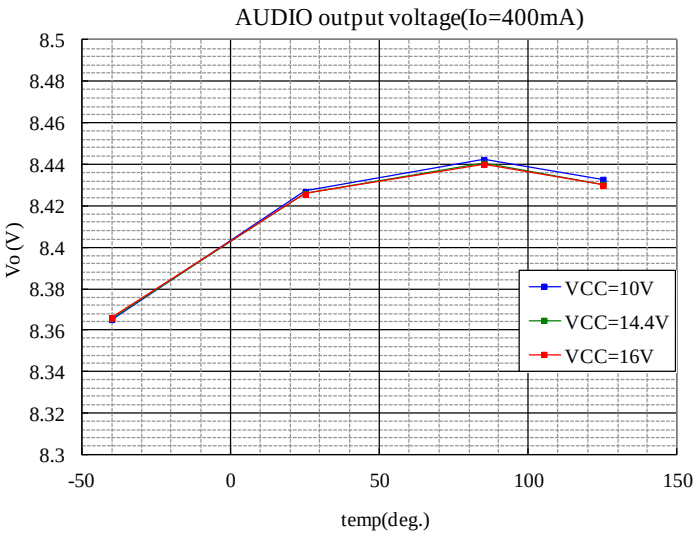


Fig29. AUDIO voltage vs Temperature

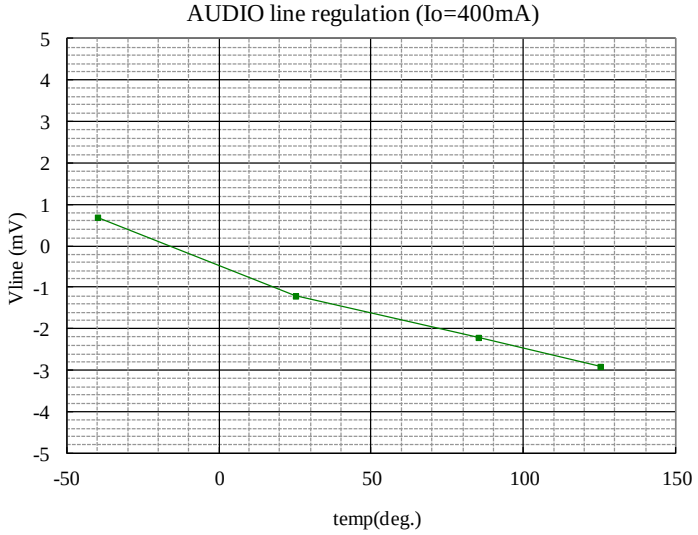


Fig30. AUDIO Line regulation vs Temperature

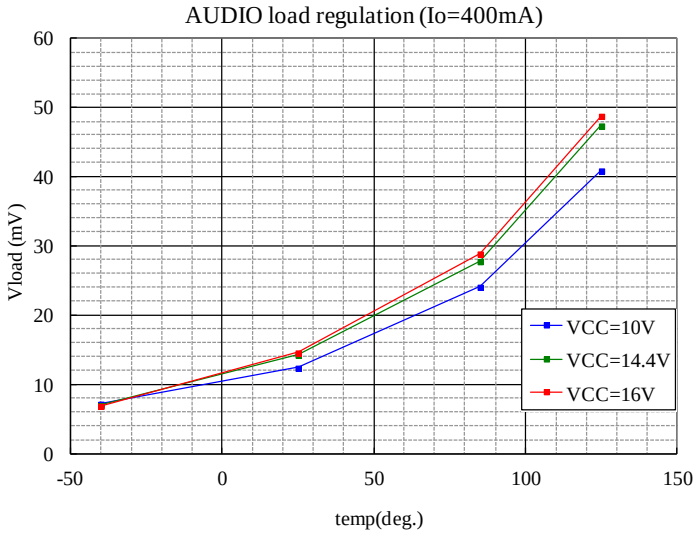


Fig31. AUDIO Load regulation vs Temperature

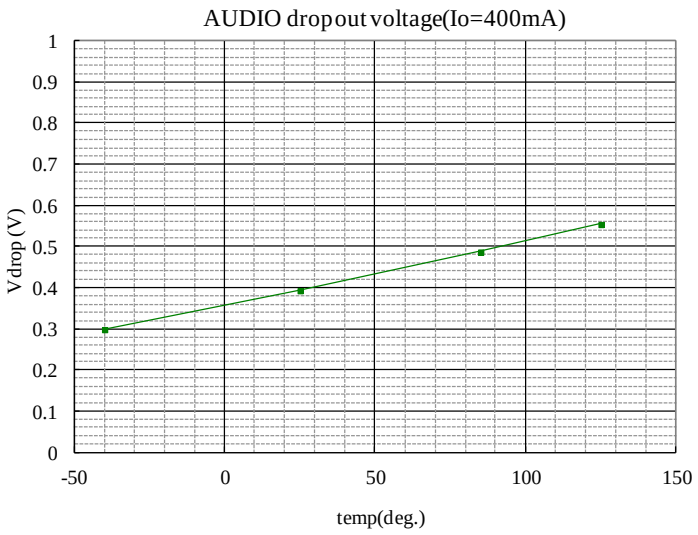


Fig32. AUDIO dropout voltage vs Temperature

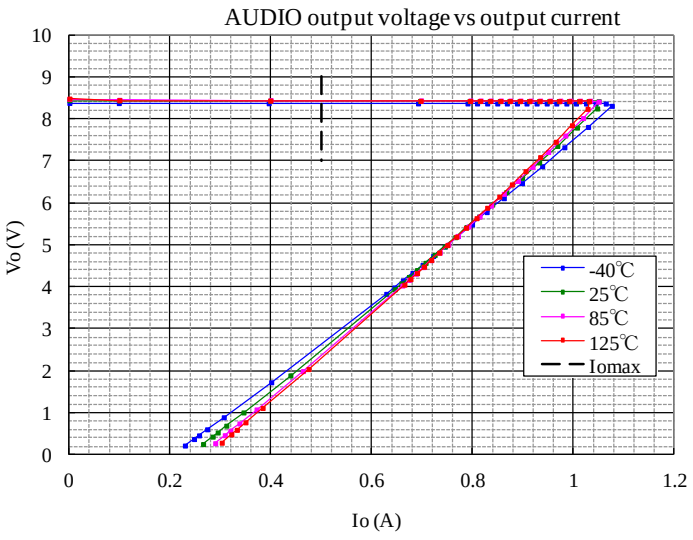


Fig33. AUDIO voltage vs current

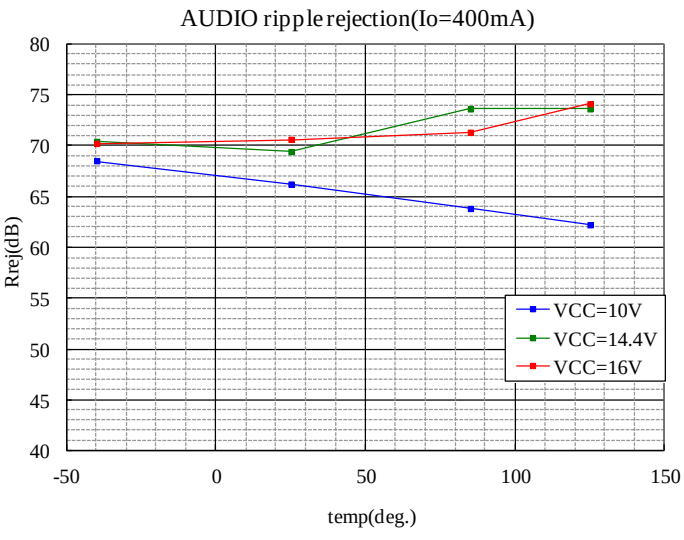


Fig34. AUDIO Ripple rejection vs Temperature

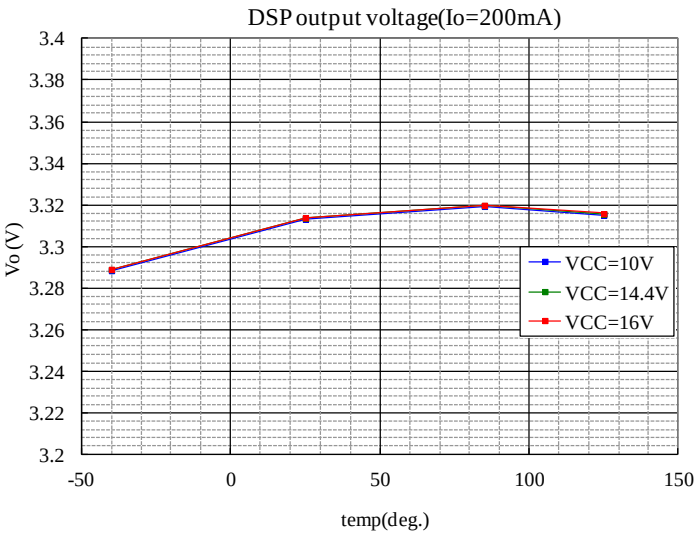


Fig35. DSP voltage vs Temperature

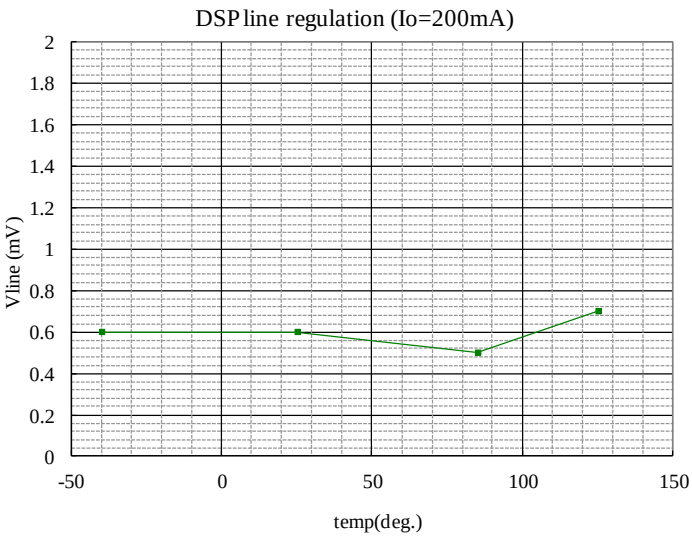


Fig36. DSP Line regulation vs Temperature

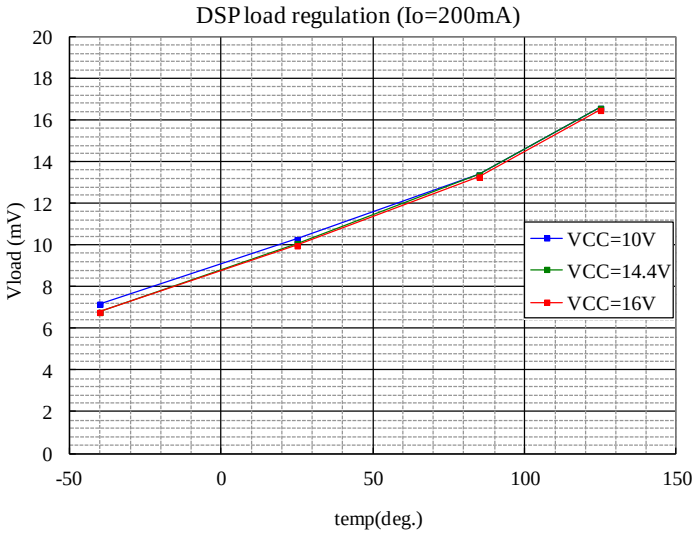


Fig37. DSP Load regulation vs Temperature

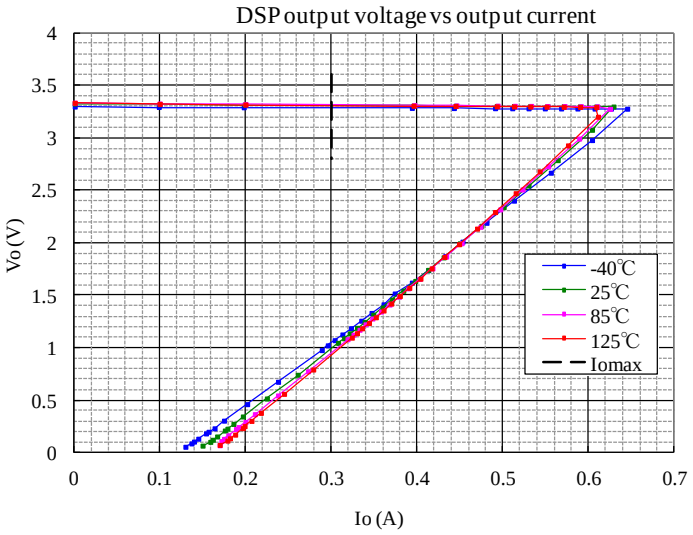


Fig38. DSP voltage vs current

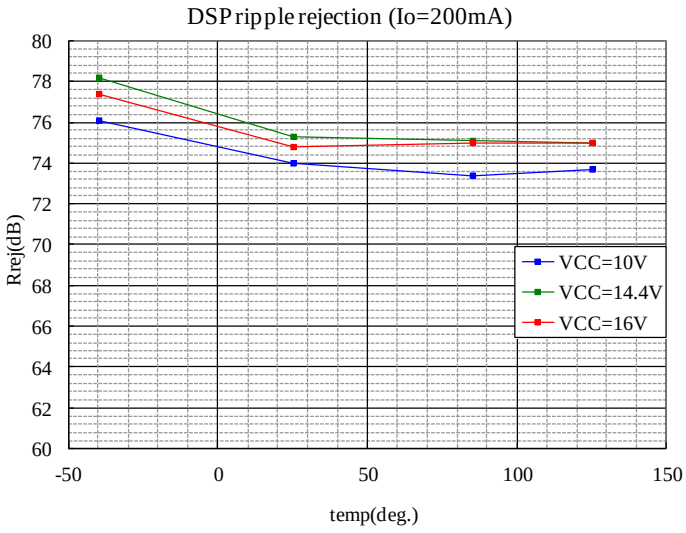


Fig39. DSP Ripple rejection vs Temperature

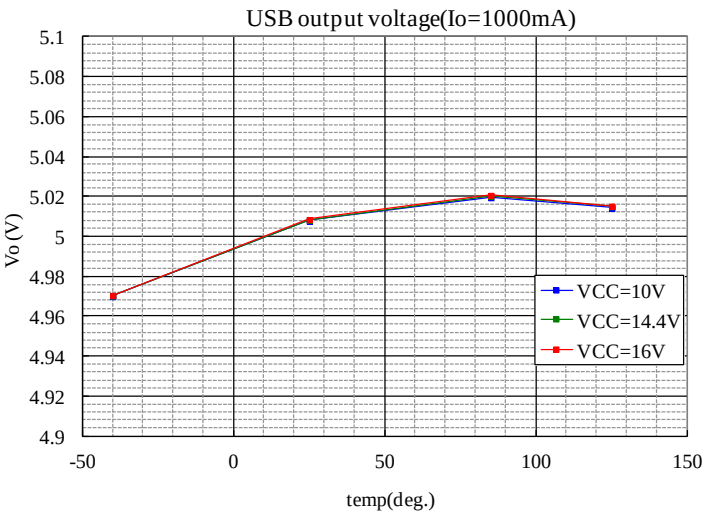


Fig40. USB voltage vs Temperature

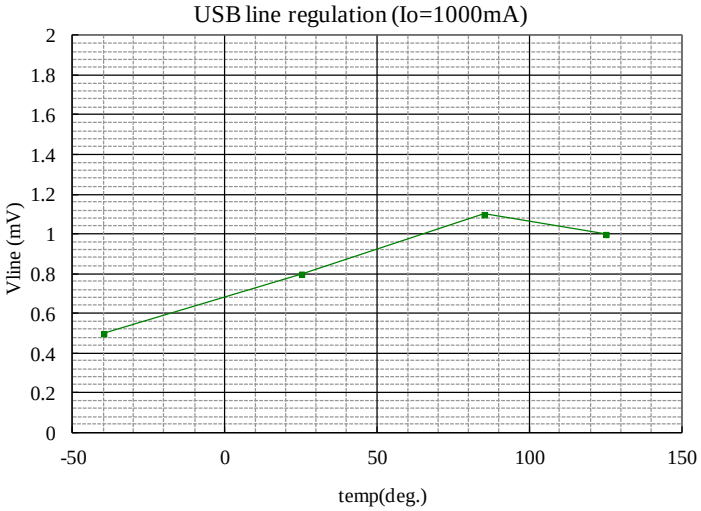


Fig41. USB Line regulation vs Temperature

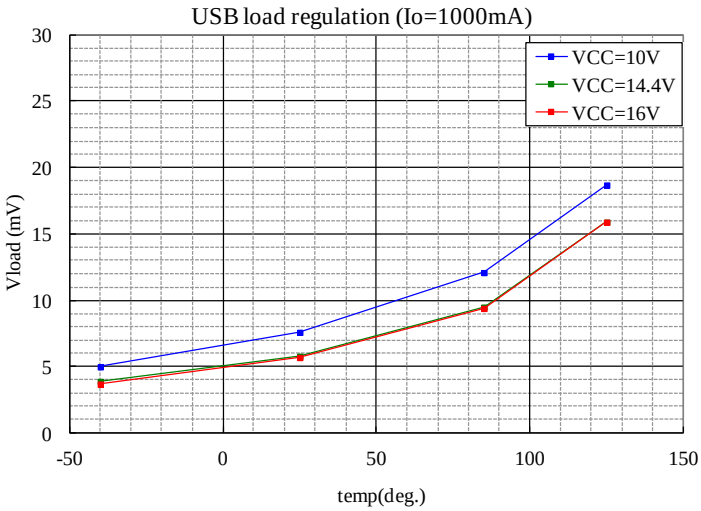


Fig42. USB Load regulation vs Temperature

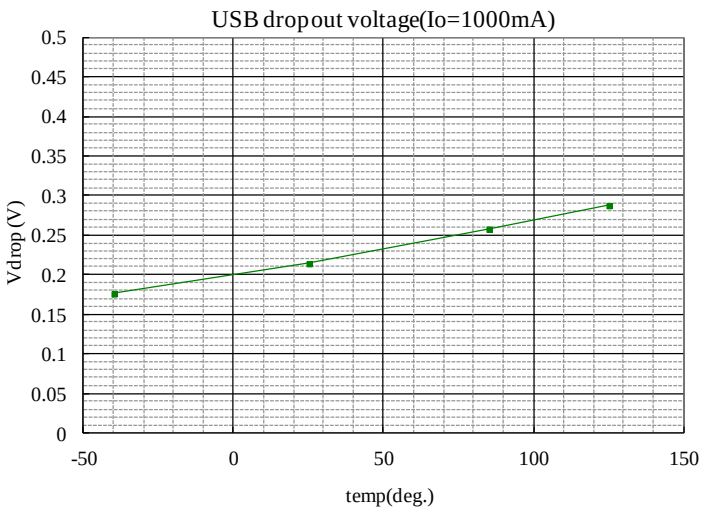


Fig43. USB dropout voltage vs Temperature

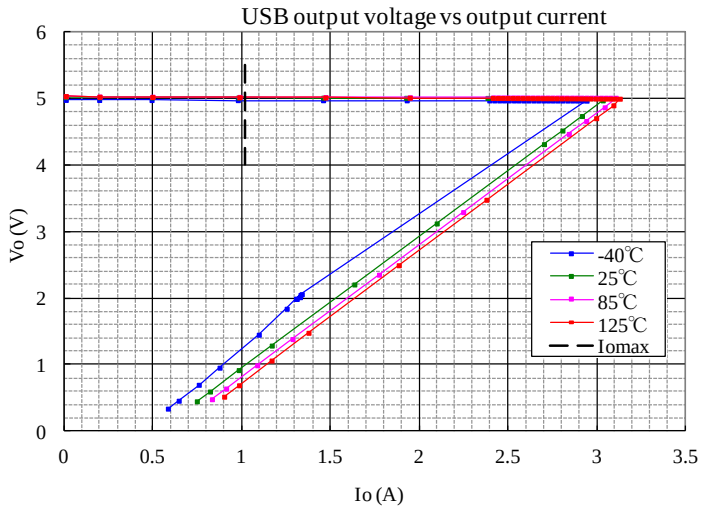


Fig44. USB voltage vs current

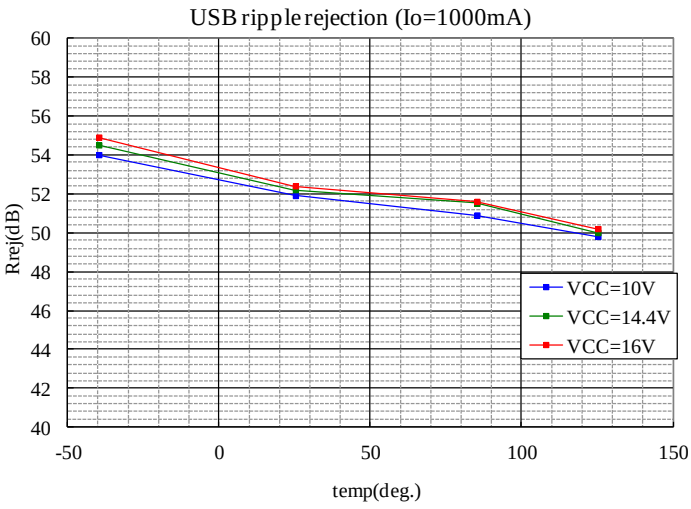
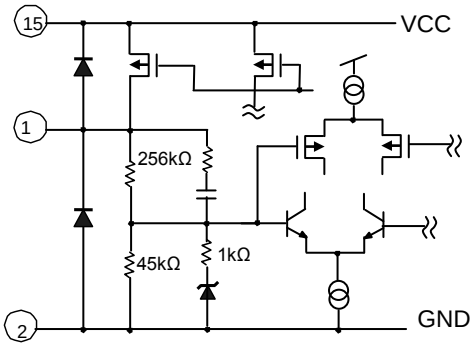
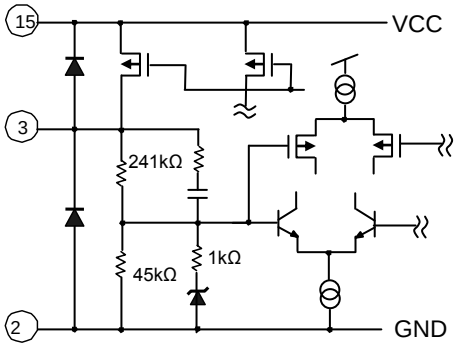
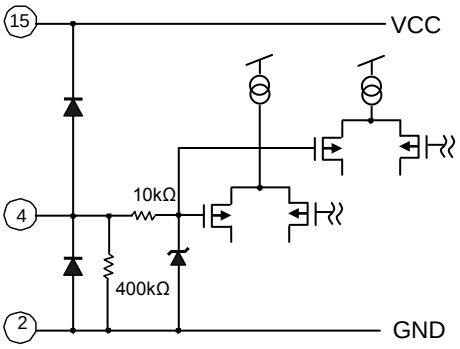
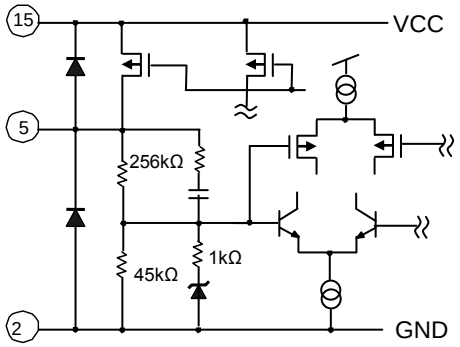
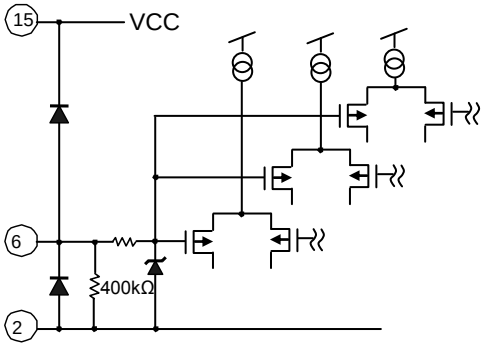
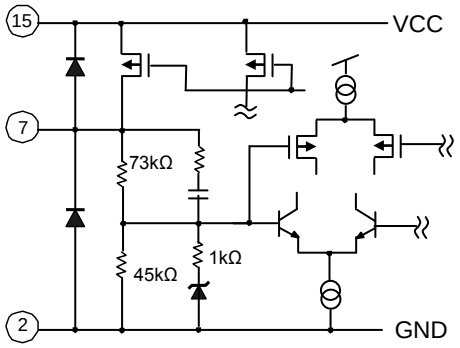
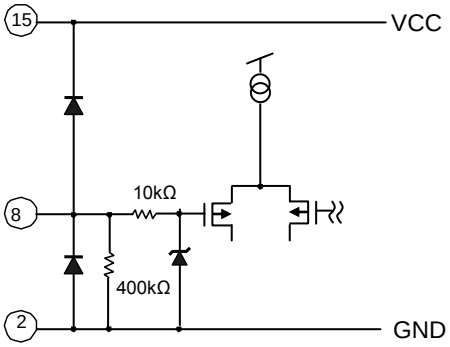
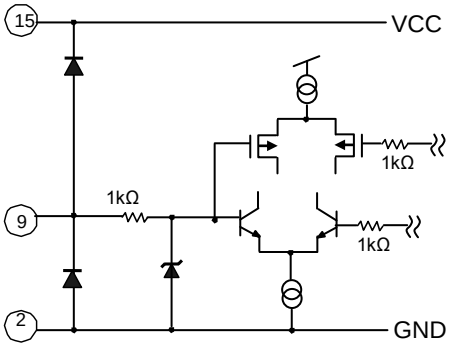
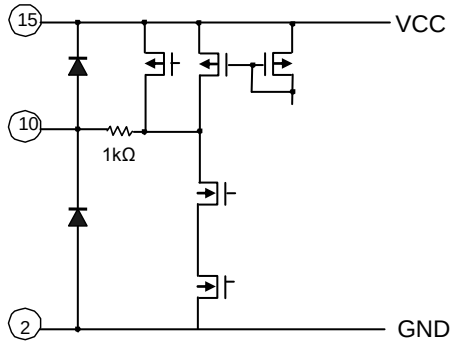
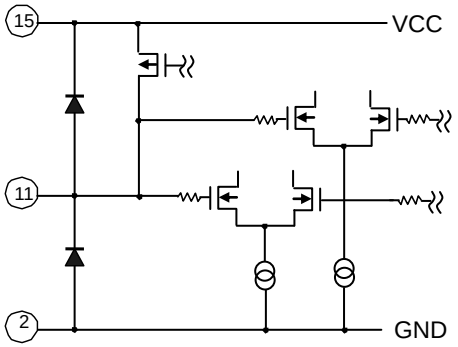
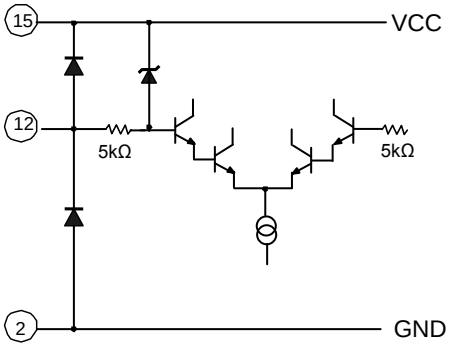
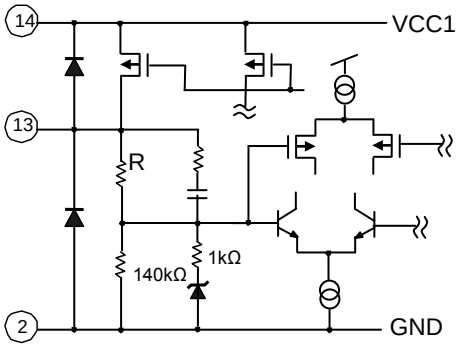
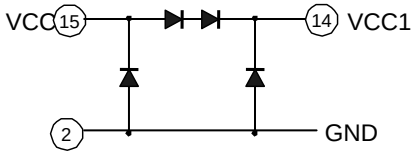


Fig45. USB Ripple rejection vs Temperature

Terminal outline

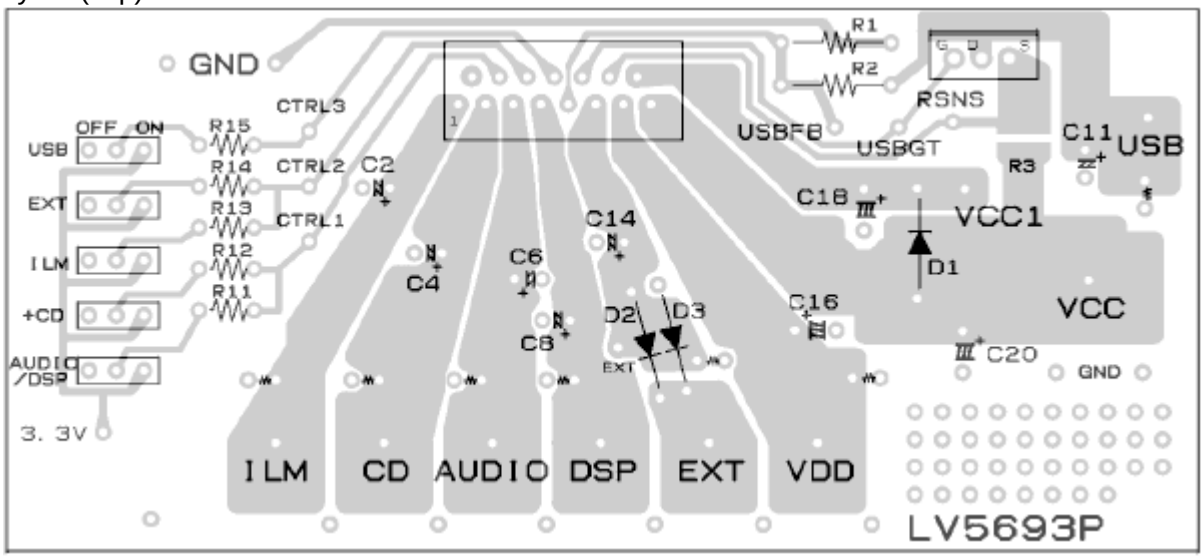
Pin No	Name	Function	Equivalent circuit
1	ILM-OUT	CTRL2=M1,H → ON 8.4V/0.5A	
2	GND	GND	
3	CD-OUT	CTRL1=H → ON 8.0V/1.3A	
4	CTRL1	CTRL1 Input pin 3 value-input	
5	AUDIO-OUT	CTRL1=M,H → ON 8.4V/0.5A	

Pin No	Name	Function	Equivalent circuit
6	CTRL2	CTRL2 Input pin 4 value-input	
7	DSP-OUT	CTRL1=M,H → ON 3.3V/0.3A	
8	CTRL3	CTRL3 Input pin 2 value-input	
9	FB	USB Feedback pin 1.26V	

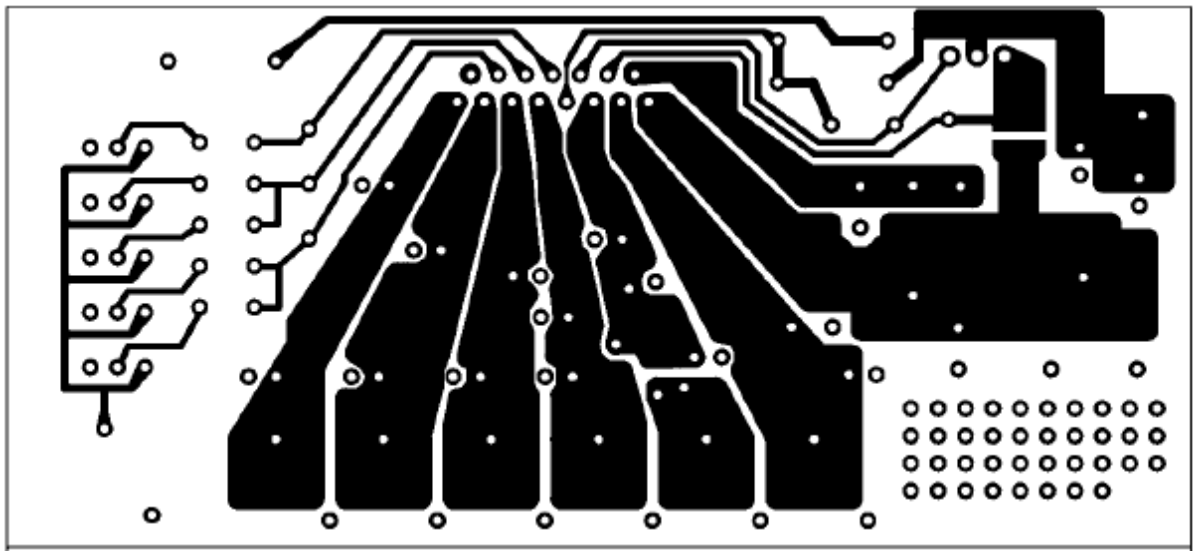
Pin No	Name	Function	Equivalent circuit
10	USBGT	Pch-FET gate drive 12.0V	
11	EXT	CTRL2=M2,H → ON VCC-0.5V/500mA	
12	RSNS	USB current detection resistor connect pin 14.3V	
13	VDD-OUT	VDD (Micon) 3.3V/0.3A:LV5692P 5.7V/0.3A:LV5693P	 R=435kΩ(LV5693P) R=240 kΩ(LV5692P)
14	VCC1	Vin for VDD	
15	VCC	Vin (B+)	

Board Layout

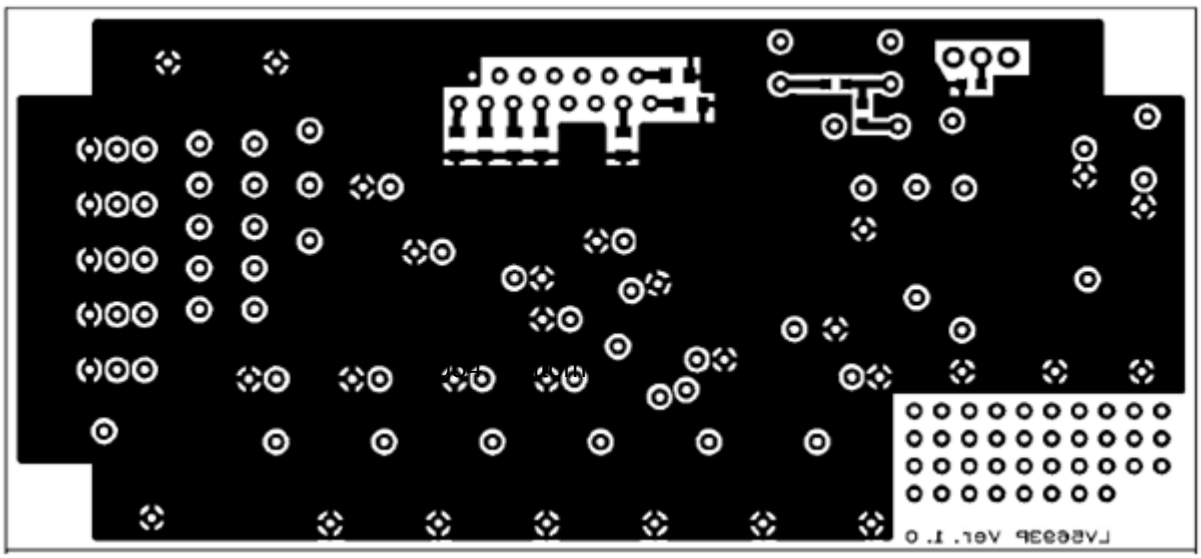
・Layer 1(Top) silk



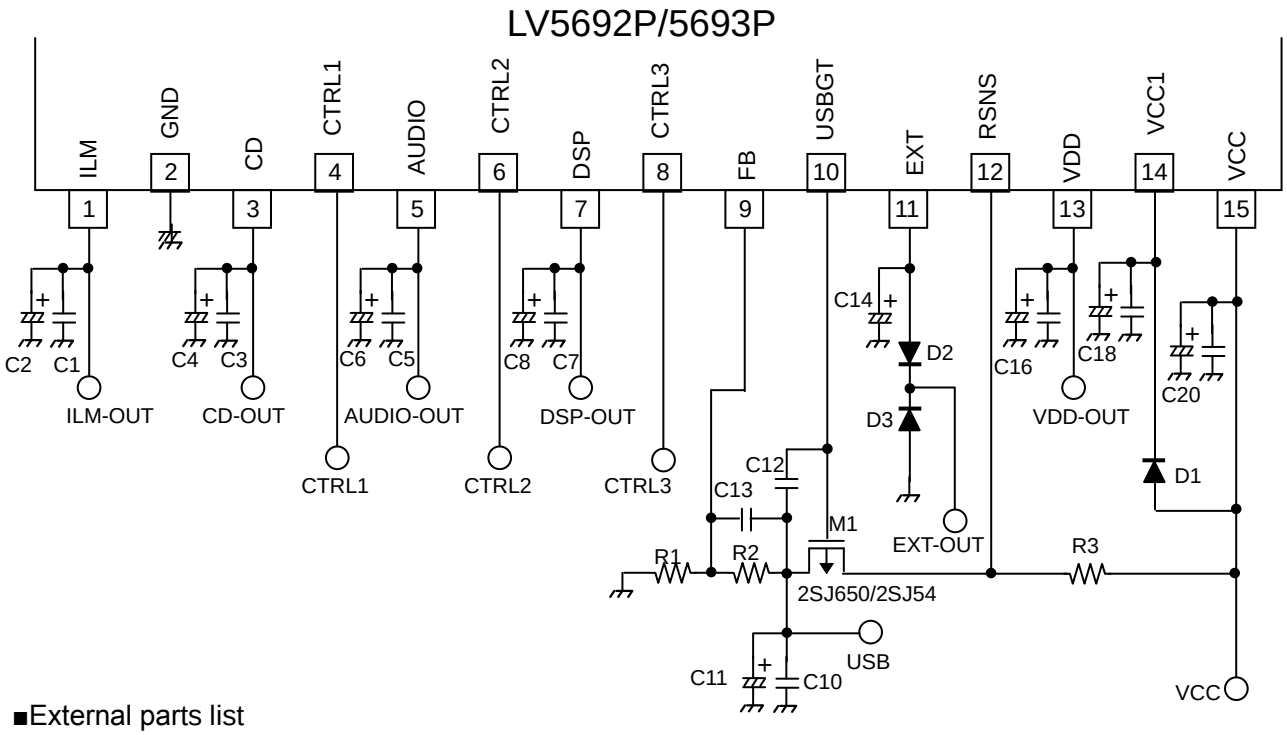
・Layer 1(Top) metal



・Layer 2(Bottom) metal



Application Circuit Example



■External parts list

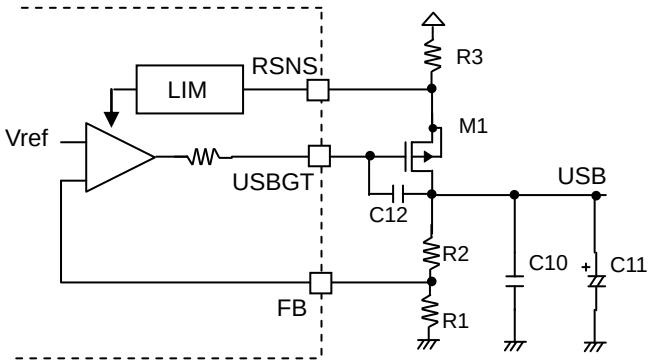
Part #	Descriptions	Recommendation value	Others
C2,C4,C6,C8,C11,C16	Output voltage stabilizer	10uF or higher (Note1)	E-cap
C1,C3,C5,C7,C10,C15	Output voltage stabilizer	0.22uF or higher (Note1)	Ceramic-cap
C12,C13	Phase compensator	C12=1000pF, (C13=0pF: TBD)	Ceramic-cap
C18,C20	By-pass	100μF or higher	Connect them close to VCC and GND
C17,C19	OSC preventers	0.22μF or higher	
C14	EXT output voltage stabilizer	2.2μF or higher	
R1,R2	USB voltage setting resistor	R1/R2=9.1kΩ/27kΩ for 5.0V	Use resistor w/ accuracy better than ±1%
R3	USB current limit setting resistor	0.1Ω for Ipeak=3A	Panasonic ERJB1CFR10U (ref)
M1	USB-OUT Pch-FET	2SJ650 (to be discontinued)	Renesas 2SJ540 SFT1342
D1	Reverse Current prevention diode		
D2,D3	IC crash preventer diode	SB1003M3	

*The circuit diagram and the values are only tentative which are subject to change.

(Note1) Make sure that the capacitors of the output pins are 10uF or higher and ESR is 10ohm or lower in total and temperature characteristics and accuracy are taken into consideration. Also the E-cap should have good high frequency characteristics.

How to set USB application

■USB block diagram



■General description

USB output is controled by CTRL3 pin.

USBGT(PIN10) is gate drive terminal of P-channel FET.

FB(PIN9) is feedback input.

RSNS(PIN12) is current sense input. When voltage difference (VCC-RSNS) exceeds 0.3V, current limits output current and foldback output voltage.

Limit current is determined by following equation. Io_lim(A)=0.3V/R3(ohm)

■Example parts list

R1,R2	USB voltage setting resistor	R1/R2=9.1kΩ/27kΩ for 5.0V	Use resistor w/ accuracy better than ±1%
R3	USB current limit setting resistor	0.1Ω for Ipeak=3A	Panasonic ERJB1CFR10U (ref)
C10	Output voltage stabilizer	0.22uF or higher (Note1)	Ceramic-cap
C11	Output voltage stabilizer	10uF or higher (Note1)	E-cap
C12,C13	Phase compensator	C12=1000pF, C13=0pF	Ceramic-cap

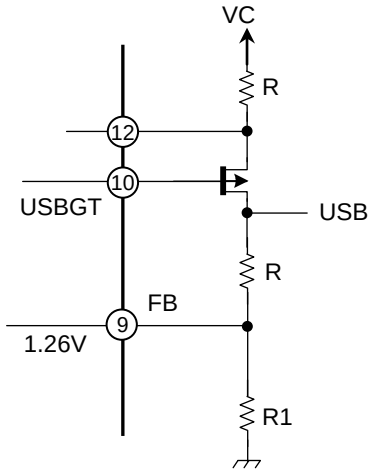
*The purpose of C12 is phase compensation of negative feedback, which guarantees regulator stability.

Recommended value range of C12 is between 470p～2000pF.

If you use the value out of the range, it causes the effect described below.

C12	advantage	disadvantage
smaller value	rapid response	lack of stability may cause oscillation
greater value	stability increase	slow transient response worse ripple rejection

・How to set USB output voltage:



(FB -voltage is defined by Vref)

USB output voltage calculation formula.

$$USB = \frac{1.26[V]}{R_1} \times R_2 + 1.26[V]$$

$$\frac{R_2}{R_1} = \frac{(USB - 1.26)}{1.26}$$

e.g. USB=5V

$$\frac{R_2}{R_1} = \frac{(5.0 - 1.26)}{1.26} \cong 2.968$$

$$\frac{R_2}{R_1} = \frac{27k\Omega}{9.1k\Omega} \cong 2.967$$

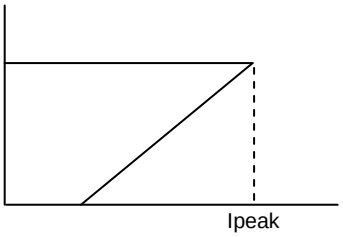
* $USB = 1.26V \times 2.967 + 1.26V \cong 4.998V$

・How to set USB over-current limit value (OCP)

OCP of the USB works when the voltage of RSNS is under “VCC-0.3V”.

The peak current value of OCP is calculated as follows:

“Ipeak (A) ＝0.3/R3” e.g. R3=0.1ohm → Ipeak=3A



(Note) The above values were obtained under typical conditions. The values have tolerance in manufacturing processes due to external resistor and IC variation.

■Thermal design

Since the controller cannot protect the FET from over-temperature damage, thermal design care must be carefully done to assure a reliable design.

The temperature of the FET and the dissipated power is defined by the equation.

■PCB layout consideration

For maximum accuracy, VCC and RSNS pins must be Kelvin connected to R3, to avoid errors caused by voltage drops along the traces carrying the current from the VCC to the Source pin of the FET.

■Warning

The internal circuits of USBGT and RSNS consist of components that support 5V. Do not bias 7V or above between VCC and these pins to prevent the IC from destruction. Do not use the device under over-voltaged condition(for example shorting these terminals to low voltage node) even for short period of time .

In normal operating condition with recommended application, the device controls voltage of these terminals within 5V.

■Application information using other FET

You can replace 2SJ650 with 2SJ540 or SFT1342 .(2SJ650 is to be discontinued.)

In case of using 2SJ540/SFT1342, value of all resisters and capacitors will be the same as the case of using 2SJ650.

Since SFT1342's package is different from that of 2SJ650/2SJ540, thermal design care must be carefully done to assure a reliable design.

You must use the FET under the condition so that the power dissipation of FET does not exceed allowable power dissipation.

Demonstration-board schematics

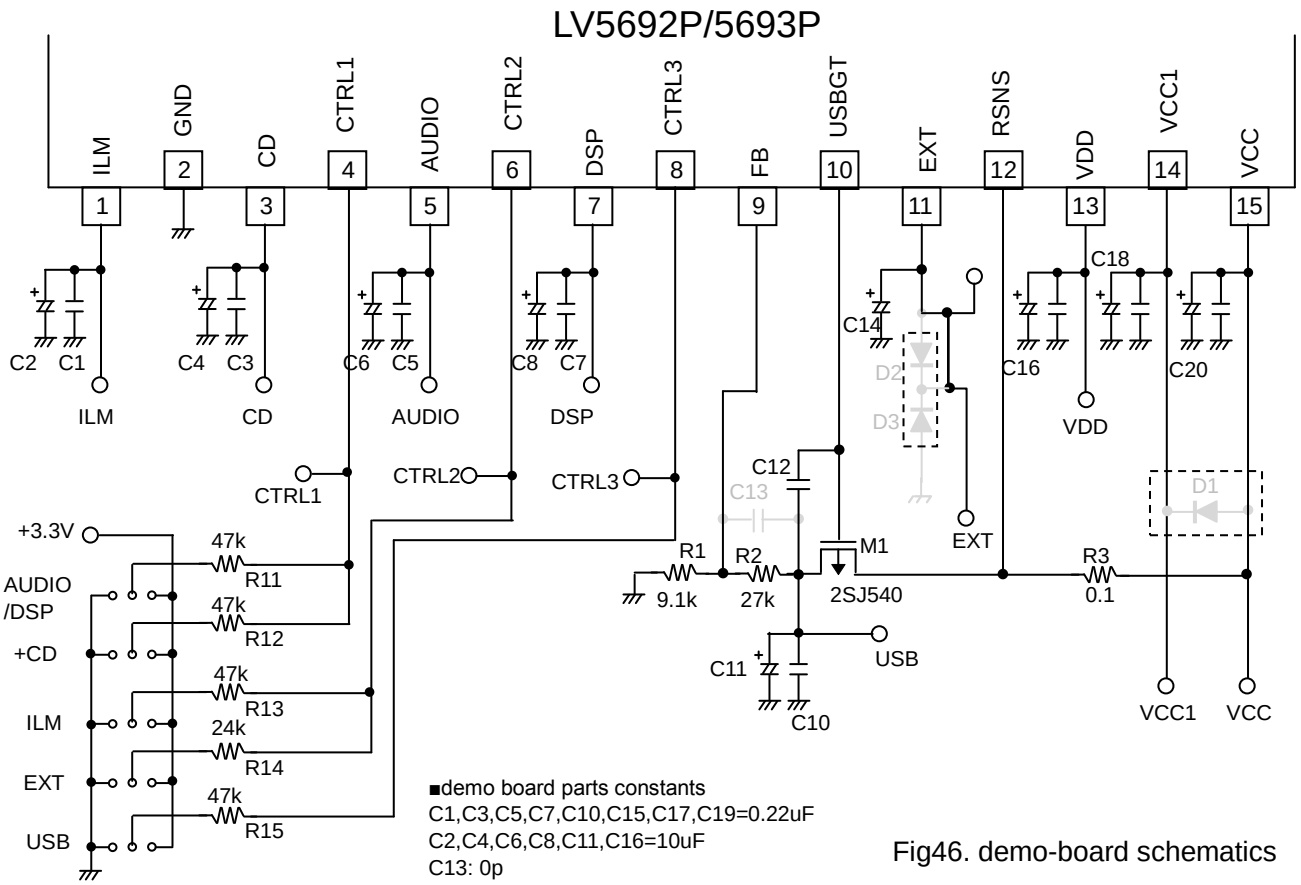
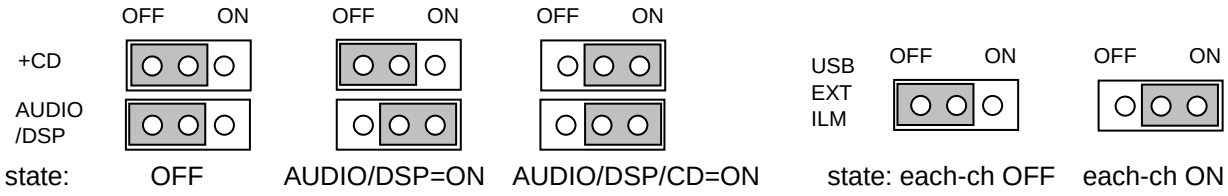


Fig46. demo-board schematics

■Jumper connector setting



・"USB" output current is from external FET. This channel has over-current limiter, but you should be careful of over heat of FET. You should consider power dissipation of FET when you determine the limit current or heat sink specification. Limit current (peak current(A)) is calculated by 0.3/R3.

Bill of Materials

Reference	Value	Part	Vendor	Comments
C18,20	100μF/50V	UVR1H101MPD	nichicon	Capacitor, Aluminum Electrolytic
C1,3,5,7,10 C15,17,19	0.22μF/50V	GRM21BR71H224KA01L	Murata	Capacitor, Ceramic
C12	1000pF/50V	GRM188R71H102KA01D	Murata	Capacitor, Ceramic
C14	2.2μF/50V	UVK1H2R2MDD	nichicon	Capacitor, Aluminum Electrolytic
C2,4,6 C8,11,16	10μF/25V	UMA1E100MDD/ ECEA1FKS100	nichicon/ Panasonic	Capacitor, Aluminum Electrolytic
R1	9.1kΩ/±1%	MF1/4CCT52A9101F	KOA	Resistor
R2	27kΩ/±1%	MF1/4CCT52A2702F	KOA	Resistor
R3	0.1Ω/1W	ERJB1CFR10U	Panasonic	Resistor, Thick Film
R11,12,13, R15	47kΩ	MFS1/4CCT52A4702F	KOA	Resistor
R14	24kΩ	MFS1/4CCT52A2402F	KOA	Resistor
M1		2SJ540-E	Renesas	P-ch power FET
BH(3pins)	3pins	W81136T3843RC	RS	Board Header
SL*		W8010T50RC	RS	Short Link
TP		ST-4-2	MAC8	Test Point

Functional Description

The LV5693P is a multiple output voltage regulator with a power switch, suitable for use in car audio system.

[Standby mode]

When all CTRL pins are "L" state (CTRL1=CTRL2=CTRL3=L), LV5692P/93P is in standby mode. In standby mode, all outputs except VDD are disabled. Quiescent current is 50uA(typ) at VDD no load. When either CTRL pin exceeds "M1" threshold voltage, LV5693P exits standby mode.

[VCC]

This IC has the tolerance value of 50V against VCC peak surge voltage, but for more safety set design, adding power clamp, such as power zenner diode, on battery connected line is recommended in order to absorb applied surge.

This IC has no protection against battery reverse connection, so adding Schottky diode is recommended to prevent a negative voltage.

[Linear Regulators]

All regulators in LV5692P/93P are low dropout outputs, because the output stage of all regulators is Pch-LDMOS.

When you select output capacitors for linear regulators, you should consider three main characteristics: startup delay, transient response and loop stability. The capacitor values and type should be based on cost, availability, size and temperature constraints. Tantalum, Aluminum electrolytic, Film, or Ceramic capacitors are all acceptable solutions. However, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but if the circuit operates at low temperatures(-25 to -40℃), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's datasheet usually provides this information.

VDD5V regulator (3.3V, 0.3A:LV5692P)
(5.7V, 0.3A:LV5693P)

When VCC is applied, VDD output is active regardless of CTRL states.

The charge on VCC1 capacitor can be used to supply VDD output for a short period when VCC voltage drops 0V.

CD regulator (8.0V, 1.3A)
AUDIO regulator (8.4V, 0.5A)
ILM regulator (8.4V, 0.5A)
DSP regulator (3.3V, 0.3A)

These regulators are controled by CTRL1/2 pins. Logic table is shown on page7.

USB regulator (5V, 1.0A)

USB output is controled by CTRL3 pin.

USBGT(PIN10) is gate drive terminal of P-channel FET.

FB(PIN9) is feedback input.

RSNS(PIN12) is current sense input. When voltage difference (VCC-RSNS) exceeds 0.3V, current limits output current and foldback output voltage.Limit current is determined by following equation.

Io_lim(A)=0.3V/R3(ohm)

For maximum accuracy, VCC and RSNS pins must be Kelvin connected to R3, to aviod errors caused by voltage drops along the traces carrying the current from the VCC to the Source pin of the FET.

For more information about USB application, refer to "How to set USB application" on page22.

[EXT high-side switches]

These are high-side power switches connected to VCC.

If these output are connected to inductive load or loads which have different ground potential, protection diodes (D2/D3) are necessary to protect the device from negative voltage.

[over current protection]

When the each output becomes in over load conditon, the device limits the output current.All outputs are also protected against short circuit by fold back current limitter.

[CTRL1/2/3 input]

CTRL1 accepts three input values (L/M/H)., CTRL2 accepts four input values(L/M1/M2/H) and CTRL3 accepts two values(L/H). CTRL1/2/3 have a pull-down resistance, and this resistance value is 400kΩ.

Logic table is shown on page7.

[VCC/VCC1]

VCC1 voltage must be higher than VCC-0.7V, because internal diode between VCC and VCC1 becomes positively biased. This internal diode cannot be used to supply current from VCC to VCC1 because this is used only for ESD protection purpose.

[Protection]

Thermal Shutdown

To protect the device from overheating a thermal shutdown circuit is included. If the junction temperature reaches approximately 175 ℃ (typ), all outputs are turned off regardless of CTRL state. Outputs remain disabled until the junction temperature drops below 145℃(typ)(automatic restoration).

The thermal shutdown circuit does not guarantee the protection of the final product because it operates out of maximum rating (exceeding Tjmax=150℃).

Current Limiting

When the each output becomes in over load condition, the device limits the output current. All outputs are also protected against short circuit by fold back current limiter.

Overvoltage

The device is protected against load dump.

When VCC voltage exceeds 21V, the device detects over voltage condition and turns all the outputs off except VDD to protect the device. If VCC voltage gets below 21V, outputs are automatically restored.

TEST Procedure

Line regulation

Line regulation is defined as the maximum change in output voltage as the input voltage is varied through the specified range. It is measured by changing the input voltage and measuring the minimum/maximum voltage of the output. Line regulation is defined as the difference between maximum and minimum voltage.

Load regulation

Load regulation is defined as the maximum change in output voltage as the load current is varied through the specified range. It is measured by changing the load current and measuring the minimum/maximum voltage of the output. Load regulation is defined as the difference between maximum and minimum voltage.

Dropout voltage

Dropout voltage is defined as the minimum input-to-output differential voltage at the specified load current required by the regulator to keep the output voltage in regulation. It is measured by reducing input voltage until the output voltage drops below the nominal value.

Ripple rejection

Ripple rejection is defined as the ratio of input ripple amplitude versus that of output.

In using LV5692P/93P, you have to check the following prior to the set design.

1. Absolute Maximum Rating (*Common notes to general semiconductor device)*

Stresses exceeding Maximum Ratings may damage the device. If stresses exceeding Maximum Ratings are applied to an IC, it might smoke or fire by the breakdown and the overheating.

We recommend derating design for reducing failure rate of device. A guide of general derating design is described below.

(1)Stress Voltage: 80% or less for Abs Max voltage.
(2)Maximum rating current: 80% or less for Abs Max Io.
(3)Temperature: 80% or less for Temperatures rating.

2. Recommended Operating Range

When Power Supply IC was used in Recommended Operating Rating and Temperature rating, IC's characteristics are guaranteed. Unless otherwise specified, we do not guarantee the specified value in all temperature ranges. As long as the IC is at operation temperature range, IC's characteristic doesn't change suddenly. Operating conditions of the input voltage and the output current are limited by the chip maximum junction temperature (Tjmax). Please decide the value of the input voltage and the output current so as not to exceed Tjmax.

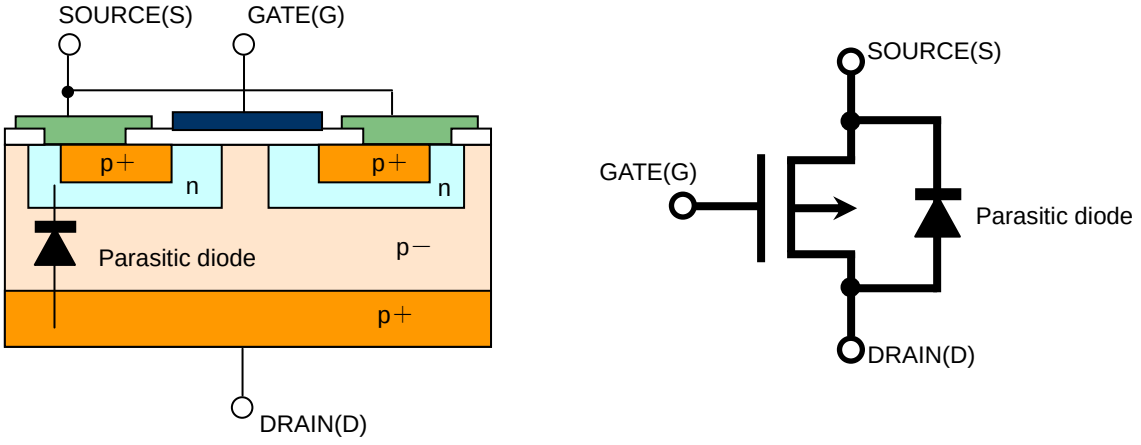
3. Output Capacitor

Between GND and each output, please be sure to put capacitor to prevent oscillation. Because abrupt changes of input voltage and output load interfere in the output voltage, make sure to use the system that will actually be offered to the market and define the output capacitor after a sufficient evaluation. When selecting the capacitor, to ensure the required minimum capacity over all operating conditions of the application, it is necessary to consider the influence of temperature and applied voltage on the capacity value.

Please design the PCB layout that the output terminal and the capacitor are located as close as possible.

4. Parasitic Devices

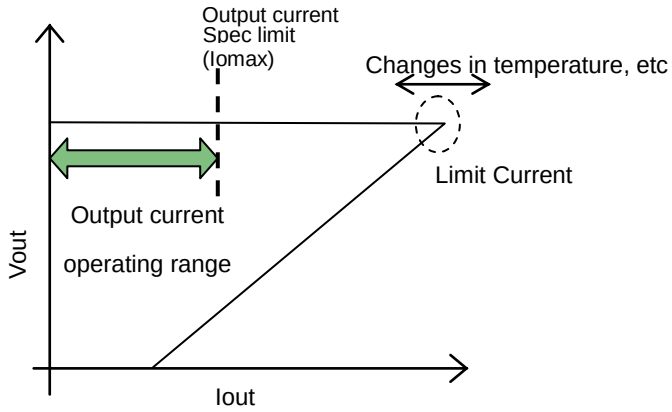
Output Power MOS-FET driver has, in device structure, parasitic diode like the figure below. Because in normal operating the input voltage is higher than the output voltage, the parasitic diode is reverse bias. If the output is higher than the input at abnormal operating, a current flows from the output to the input, because the parasitic diode is forward biased.

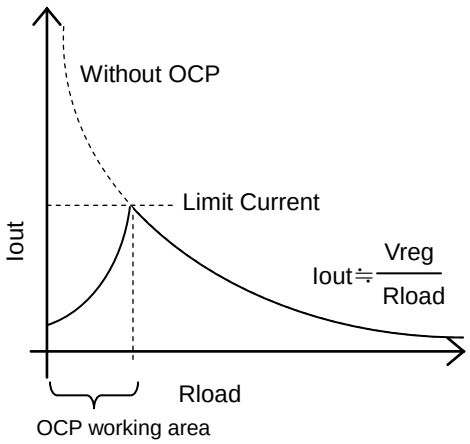


5. Over -Current Protection

Each channel has an Over-Current Protection (OCP) circuit which is the "Fold-Back" type, OCP circuit prevent IC's break down at an over current condition. This circuit is useful against sudden over current, but use of continuous operation is not allowed.

The limit value of output current is changed by ambient temperature and production tolerance. However, the limiting value doesn't fall below the output maximum current defined by the specification. When you use the output current exceeding the maximum current, the OCP circuit might operate in some situations. Be sure to design the equipment, so that the output current is below a specified maximum value.





6. Over-Voltage Protection

When VCC voltage exceeds 21V, the device detects over voltage condition and shuts down all output except "VDD" to protect the device.

The peak voltage value (Vcc peak) changes depending on Surge-waveform condition. Adding power clamp, such as power zenner diode, on battery connected line is recommended in order to absorb applied surge.

7. Thermal shut-down

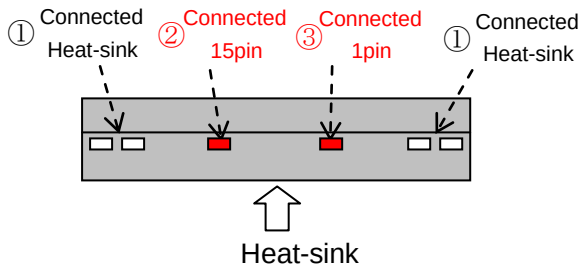
This IC has built-in thermal shut-down circuit to prevent from thermal damage. If the chip temperature (Junction temperature:Tj) reaches 175℃, the thermal shut-down circuit operates. When the thermal shut-down circuit operates, all outputs are turned off regardless of CTRL state. Outputs remain disabled until the junction temperature drops below 145℃(typ)(automatic restoration). If the operating condition is not changing, the output repeats on and off. The output seems to oscillate.

* The protector functions only improve the IC's tolerance and they do not guarantee the safety of the IC if used under the conditions out of safety range or ratings. Use of the IC such as use under over-current protection range or thermal shutdown state may degrade the IC's reliability and eventually damage the IC.

8. Notes on Installation

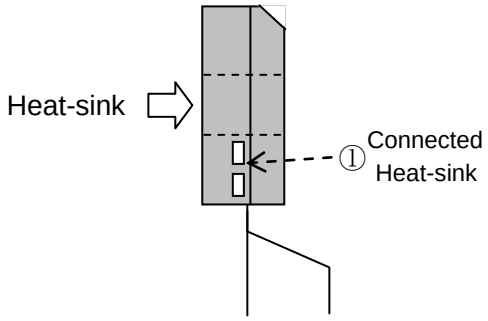
Package "HZIP15J", there are some places where metal is exposed except terminals and a heat sink. This includes the one connecting with the function pin. Especially, when you mount hardware covers over the IC, do not bring “②” & ”③” (in below figure) into contact with mounting hardware. The potential of point “①” as well as the heat sink is equal to GND.

・HZIP15J



▭ : Expose metal part

＜HZIP15J Top view＞

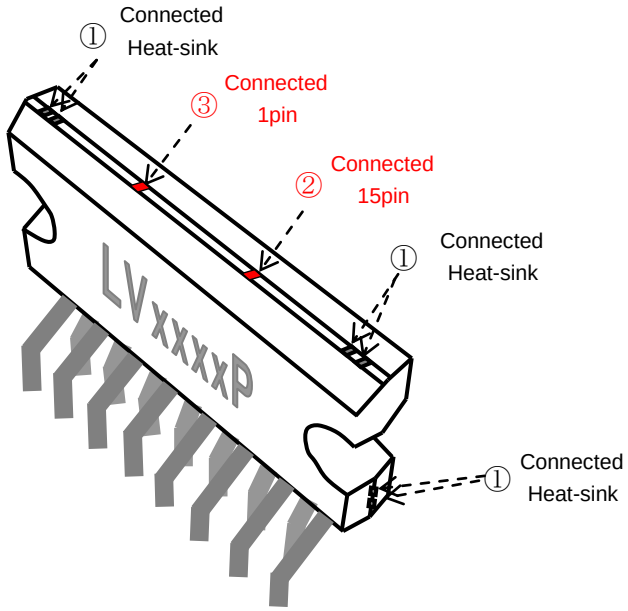


▭ : Expose metal part

※Same as other side

＜HZIP15J Side view＞

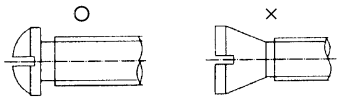
*Caution :Do not bring “②” & ”③” into contact with mounting hardware.



HZIP15J　Heat sink attachment

Heat sinks are used to lower the semiconductor device junction temperature by leading the head generated by the device to the outer environment and dissipating that heat.

a . Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.



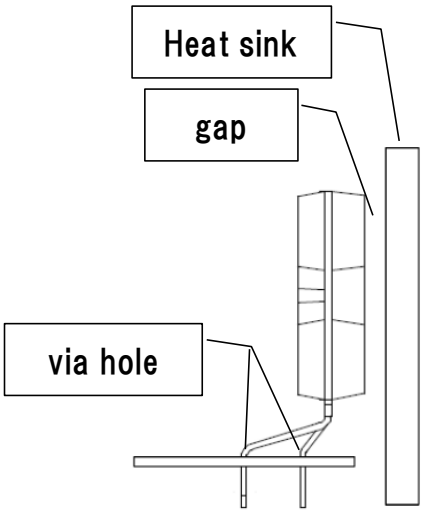
Binding-head machine-screw　　Countersunk head machine screw

b . Heat sink attachment

- Use flat-head screws to attach heat sinks.
- Use also washer to protect the package.
- Use tightening torques in the ranges 39-59Ncm(4-6kgcm) .
- If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
- Do not **make gap**, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- take care a position of via hole.
- Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- Verify that there are no press burrs or screw-hole burrs on the heat sink.
- Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
- Twisting　must be limited to under 0.05 mm.
- Heat sink and semiconductor device **are mounted in parallel**.

Take care of electric or compressed air drivers

- The speed of these torque wrenches should never exceed 700 rpm, and should typically be about 400 rpm.



c. Silicone grease

・Spread the silicone grease evenly when mounting heat sinks.

・Our company recommends YG-6260 （ Momentive Performance Materials Japan LLC ）

d. Mount

・First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.

・ When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.

e. When mounting the semiconductor device to the heat sink using jigs, etc.,

・Take care not to allow the device to ride onto the jig or positioning dowel.

・Design the jig so that no unreasonable mechanical stress is not applied to the semiconductor device.

f. Heat sink screw holes

・Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.

・ When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.

・ When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.

g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.

9. Application Circuit Example

IC’s operating characteristics are influenced by PCB layout, connection, parasitic capacitance and inductance. Therefore, make sure to use the system that will actually be offered to the market and define a constant after a sufficient evaluation.

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